



# B75H2-AM-DNI

Rev :A

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### NOTE:

Design by  
473718 Maho Bay and Carlow-WS Platforms - Design Guide - Rev. 1.5,  
474146 Panther\_Point\_EDS\_Rev1.5  
MahoBay\_CRB\_Rev0.7

## REVISION HISTORY:

Rev	Date	Notes
V.A	2012/01/02	Initial version

Table 1-2. Desktop Panther Point Chipset SKUs

Feature Set	SKU Name					
	Q77	Q75	B75	Z77	Z75	H77
PCI Express* 2.0 Ports	8	8	8	8	8	8
PCI Interface	Yes	Yes	Yes	No <sup>3</sup>	No <sup>3</sup>	No <sup>3</sup>
Total number of USB ports	14	14	12 <sup>4</sup>	14	14	14
• USB 3.0 Capable Ports (SuperSpeed and all USB 2.0 speeds)	4	4	4	4	4	4
• USB 2.0 Only Ports	10	10	8	10	10	10
Total number of SATA ports	6	6	6	6	6	6
• SATA Ports (6 Gb/s, 3 Gb/s, and 1.5 Gb/s)	2 <sup>5</sup>	1 <sup>6</sup>	1 <sup>6</sup>	2 <sup>5</sup>	2 <sup>5</sup>	2 <sup>5</sup>
• SATA Ports (3 Gb/s and 1.5 Gb/s only)	4	5	5	4	4	4
HDMI/DVI/VGA/DisplayPort*/eDP*	Yes	Yes	Yes	Yes	Yes	Yes
Integrated Graphics Support	Yes	Yes	Yes	Yes	Yes	Yes
Intel® Rapid Storage Technology	AHCI	Yes	Yes	Yes	Yes	Yes
	RAID 0/1/5/10 Support	Yes	Yes <sup>7</sup>	No	Yes	Yes
	Intel® Smart Response Technology	Yes	No	No	Yes	No
Intel® Anti-Theft Technology	Yes	Yes	Yes	Yes	Yes	Yes
Intel® Active Management Technology 8.0	Yes	No	No	No	No	No
Intel Fast Flash Standby <sup>8</sup>	Yes	No	No	No	No	No

### NOTES:

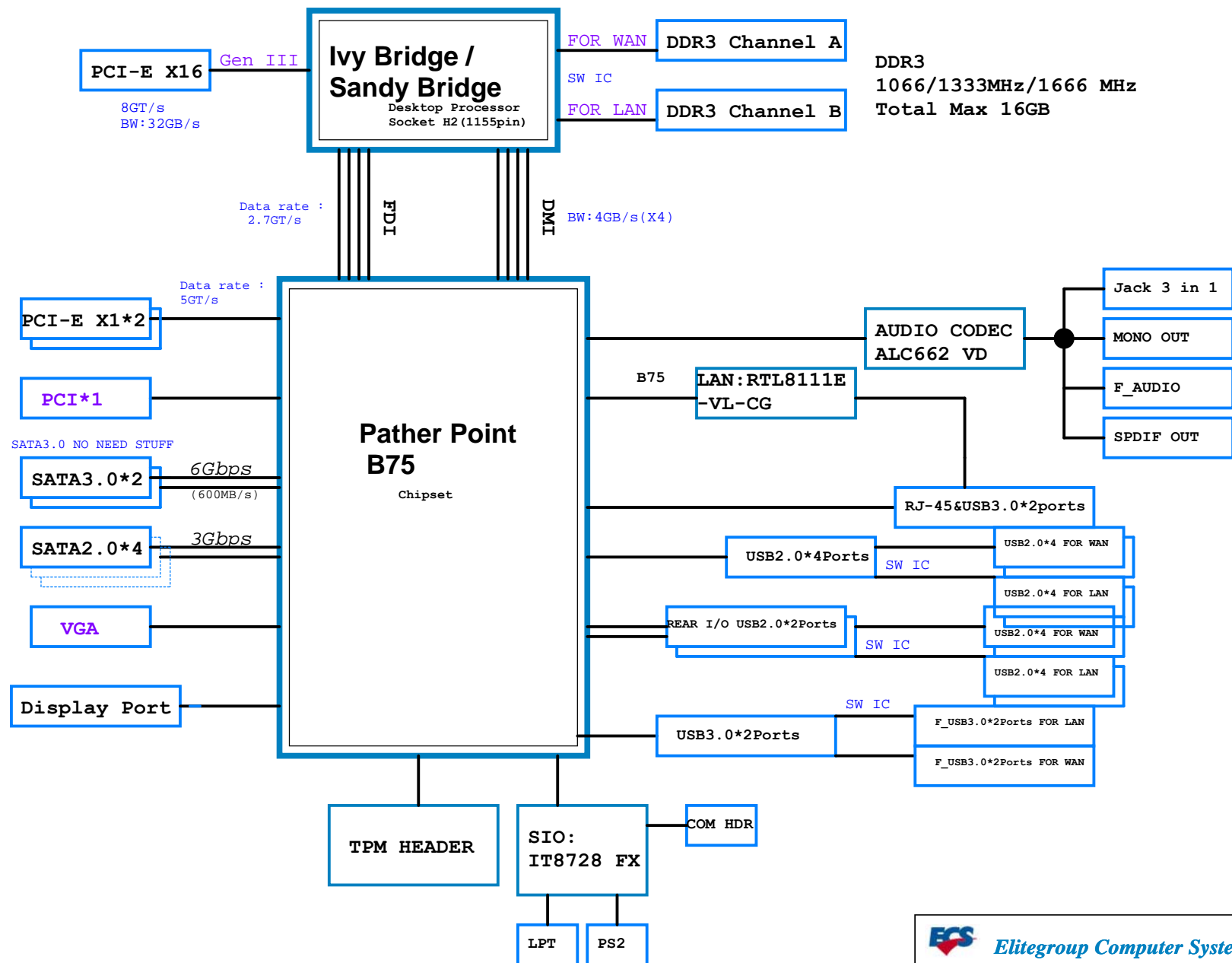
1. Contact your local Intel Field Sales Representative for currently available PCH SKUs.
2. Table above shows feature differences between the PCH SKUs. If a feature is not listed in the table it is considered a Base feature that is included in all SKUs.
3. PCI Legacy Mode may optionally be used allowing external PCI bus support through a PCIe-to-PCI bridge. See Section 5.1.9 for more details.
4. USB ports 6 and 7 are disabled.
5. SATA 6 Gb/s support on port 0 and port 1. SATA ports 0 and 1 also support 3 Gb/s and 1.5 Gb/s.
6. SATA 6 Gb/s support on port 0 only. SATA port 0 also supports 3 Gb/s and 1.5 Gb/s.
7. Supports RAID 1 only.
8. Intel Fast Flash Standby naming is not final at this time and is subject to change.



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## PCH-GPIO function

Pin Name	Power Well	Usage	Default Status
GPIO1	VCC3	OBR	GPI
GPIO6	VCC4	Over_temp	GPI
GPIO12	3VSB	LAN_DISABLE_L	Native
GPIO13	3VSB	LPC_PME_L	GPI
GPIO23	VCC3	HDPANEL_DETECT	Native
GPIO24	3VSB	OE_L DETECT	GPI
GPIO27	SB_3VSB	DEEP LANWAKEB	GPI
GPIO45	3VSB	SPI_WPSW	Native
GPIO57	3VSB	SPI_WP0_L	GPI
GPIO59	3VSB	LAN_LED_D	Native
GPIO61	3VSB	LPCPD_L	Native
GPIO72	3VSB	F_USB3 Power Control	GPO
GPIO44	3VSB	FOR ACER GPIO	GPI
GPIO46	3VSB	FOR ACER GPIO	GPI

## SIO-GPIO function

Pin Name	Power Well	Usage	Default Status
GPIO14		Over_temp	
GPIO34		MB_ID1	
GPIO16		SIO_BEEP	
GPIO22		SIO_LED1	
GPIO23		SIO_LED0	
GPIO35		MB_ID2	
GPIO36		NET_SEL	
GPIO40		5VDAUL_MEM Control	
GPIO64		MODE_SEL	
GPIO47		TP_VGA	
GPIO41		SEL1 DETECT	

### Straping Table

#### FCH Straping (Page.14)

##### TLS Confidentiality:

TLS_EN (internal PD)	
H	Enable TLS
L	Disable TLS

##### No Reboot:

FCH_SPKR (internal PD)	
H	Enable No Reboot
L	Disable

##### On-Die PLL VR:

ON_DIE_PLL_EN (internal PU)	
H	Enable
L	Disable

##### On-Die PLL VR Source:

HDA_SYNC_R (internal PD)	
H	1.5V
L	1.8V

##### Integrated 1.05V SUS VRM:

INTVRMEN	
H	Enable
L	Disable

### SIO IT8728F D/EX/FX Straping (Page.26)

#### Power-On Strapping

	Symbol	Value	Description
JP1	DSW_EUP_SEL	1	EUP
Pin-48		0	DSW
JP2	WDT_EN	1	Disable WDT to reset PWROK
Pin-122		0	Enable WDT to reset PWROK
JP3	FAN_CTL_SEL	1	EC Index 63h/6Bh/73h is 80h
Pin-124		0	EC Index 63h/6Bh/73h is 00h
JP4	K8PWR_EN	1	Disable K8 Power Sequence
Pin-126		0	Enable K8 Power Sequence
JP5	UOVMODE_SEL	1	Notice Mode (Default)
Pin-29	OV/UV	0	Force Mode

\* Port 1 or Port 9 is USB 2.0 Debug Port

### Panther point INT# Table

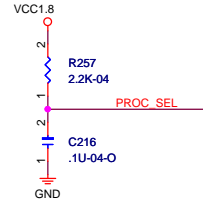
Function	INT Port	PCI-EX1 Port	Chip
Lan Ethernet Controller	INTC# (Default)	Port3	Intel 82579LM / Realtek RTL8111E
SATA 1&2 Controller (IDE Mode)	INTB# (Default)	NA	PCH intergrated
PCIEX Slot	INTD# (Default)	Port4	External PCIEX Card



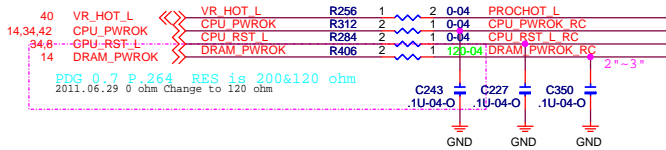




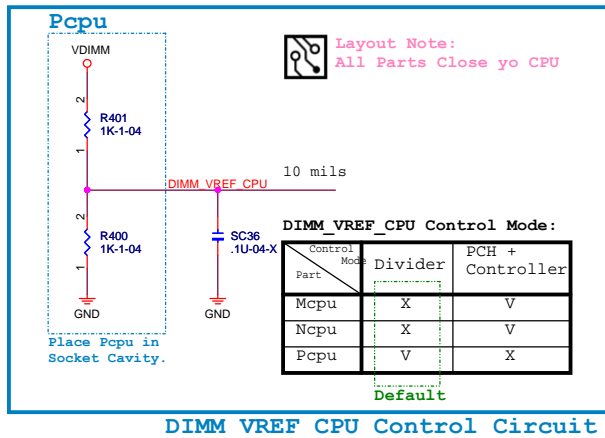
DMI/FDI TERMINATION VOLTAGE  
 DC COUPLED: TX/RX TO VCC ISF SAMPLED HIGH  
 DC COUPLED: TX/RX TO VSS IF SAMPLED LOW  
 AC COUPLED: TX SET TO VCC/2, RX SET TO VSS REGARDLESS OF THIS STRAP



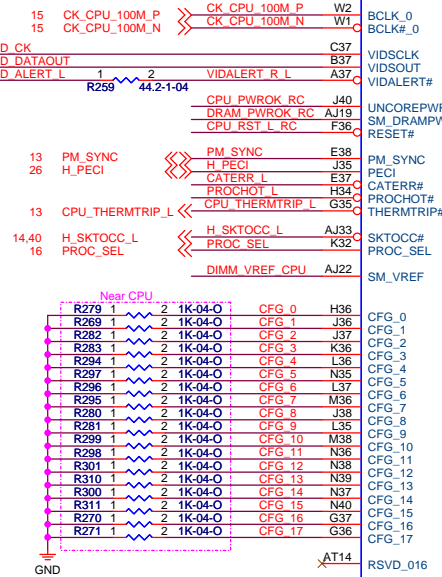
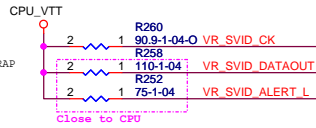
34 CFG\_0 << CFG\_0  
 To Hook2 for PDG Require



2011.09.10 Remove Divider Control Circuit



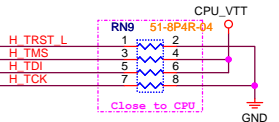
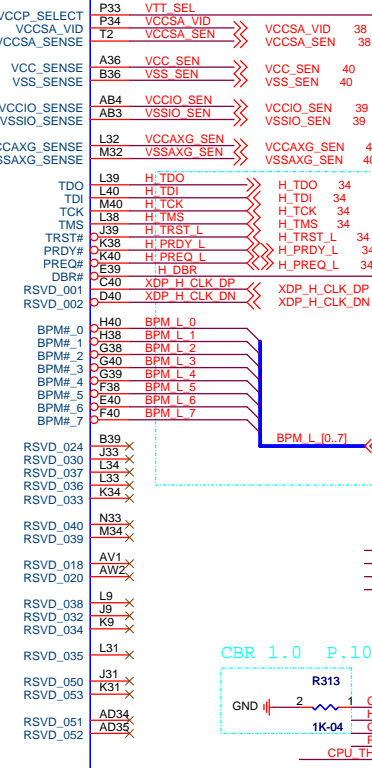
DIMM\_VREF\_CPU Control Circuit



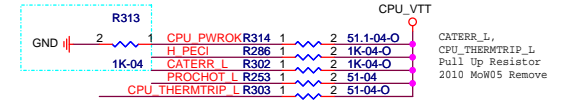
BALLMAP\_REV=1.4

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SKT\_H2\_CRB



CBR 1.0 P.10



CFG	H	L	DESCRIPTION
0	reserved	reserved	reserved
1	reserved	reserved	reserved
2	NORMAL	REVERSE	PEGLANE REVERSAL[0] X16
3	reserved	reserved	reserved
4	reserved	reserved	reserved
5	*	*	PEOF GSEL[0]
6	*	*	PEOF GSEL[1]
7	reserved	reserved	reserved
8	reserved	reserved	reserved
9	reserved	reserved	reserved
10	reserved	reserved	reserved
11	reserved	reserved	reserved
12	reserved	reserved	reserved
13	reserved	reserved	reserved
14	reserved	reserved	reserved
15	reserved	reserved	reserved

CFG [0..17] HAVE INTERNAL PULL-UPS

PCIE CONFIG	SELO	SEL1
1 X 16	1	1
2 X 8	0	1

CFG[5:6]:  
 11=DEFAULT X16,  
 01=2X8,  
 10=RESERVED,  
 00=X8,X4,X4

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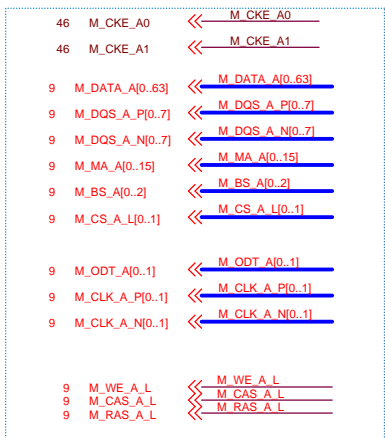
**CPU - MISC**

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Date: Wednesday, February 01, 2012

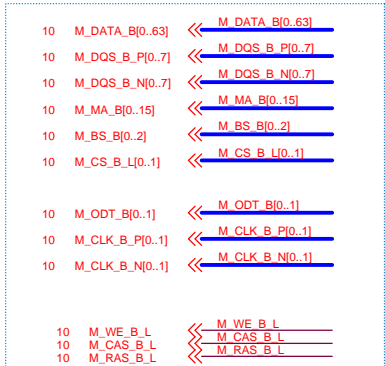
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DDR3 CH.A

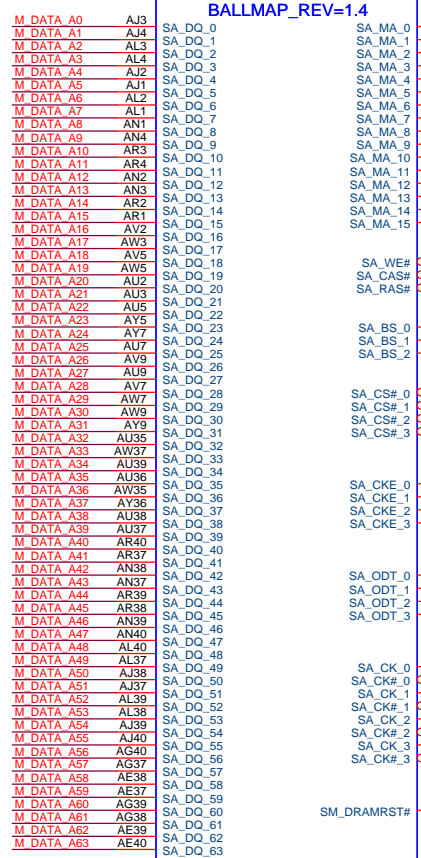
46 DDR3\_DRAMRST\_L << DDR3\_DRAMRST\_L



DDR3 CH.B

46 M\_CKE\_B0 << M\_CKE\_B0

46 M\_CKE\_B1 << M\_CKE\_B1



SM\_DRAMRST#

SA\_DQS\_8

SA\_ECC\_CB\_0

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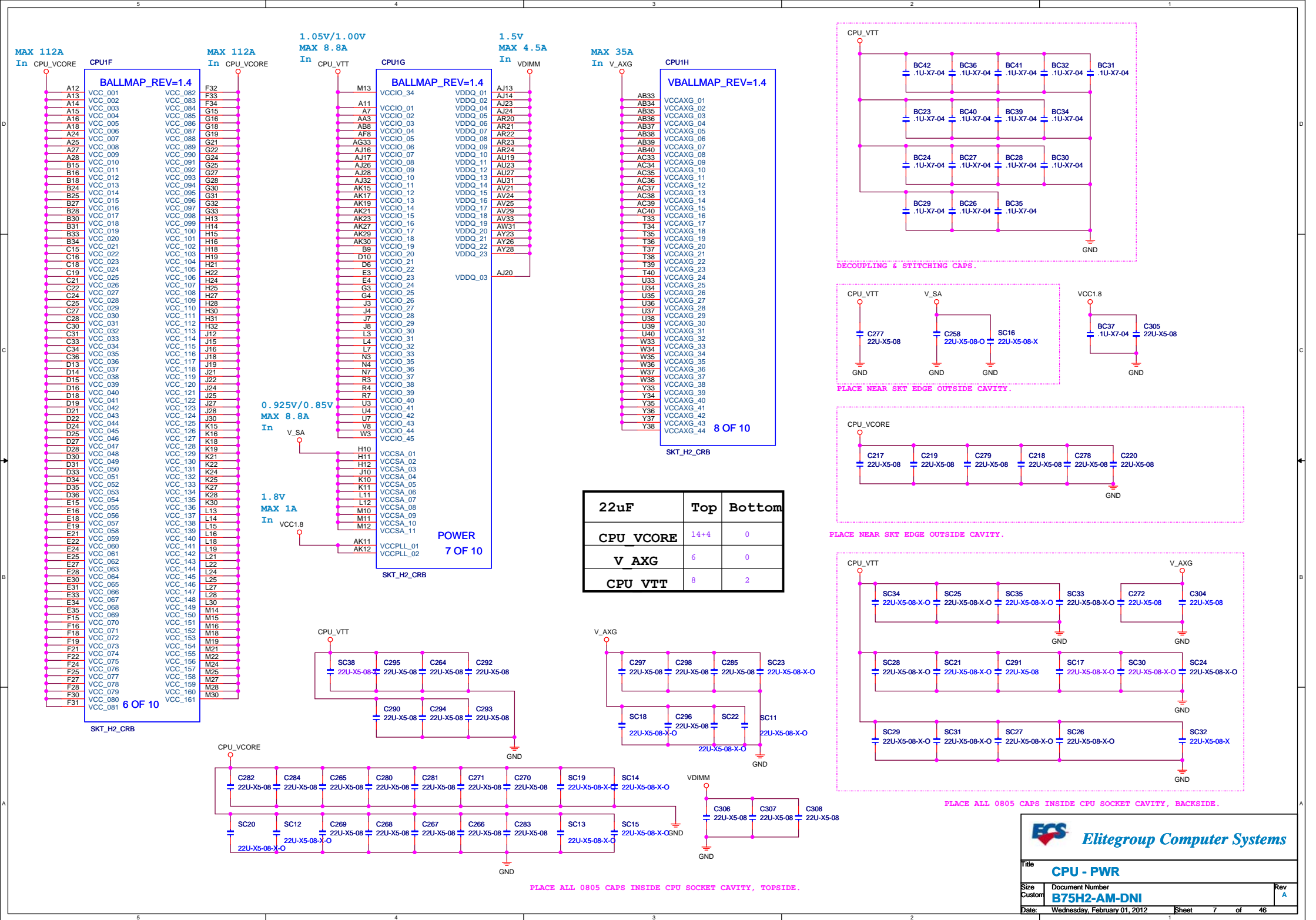
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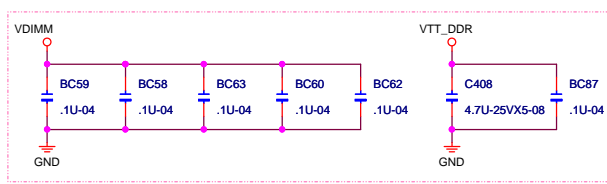
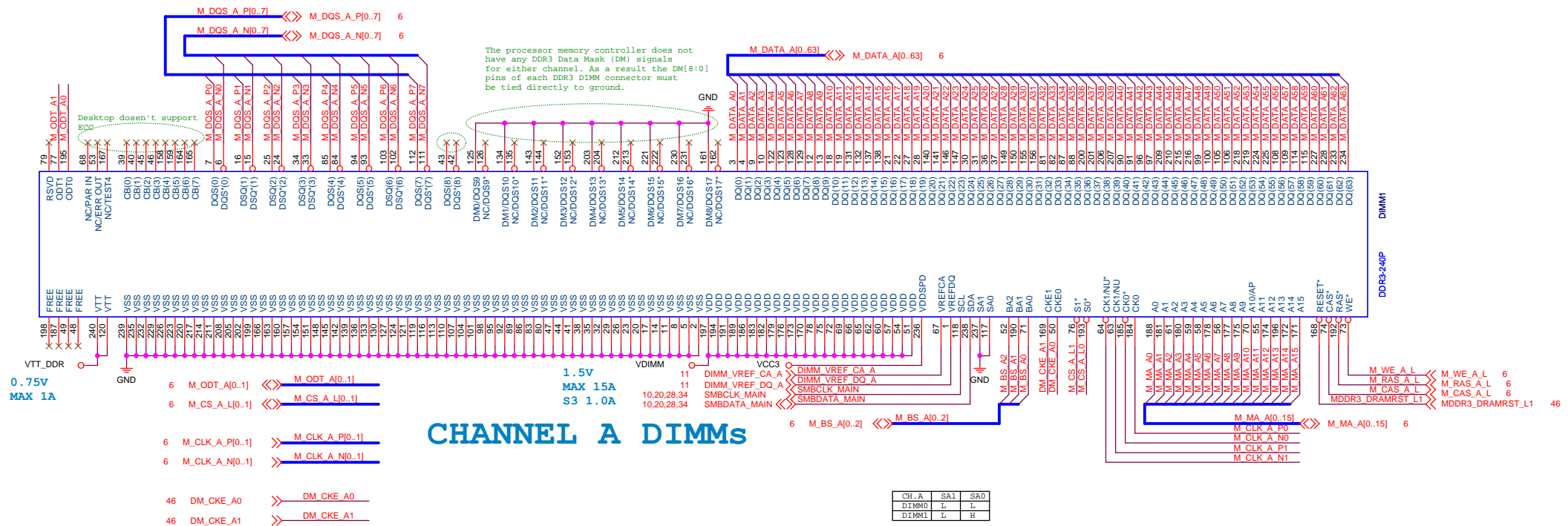




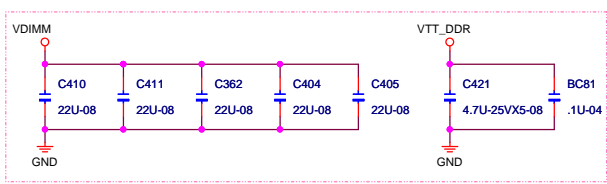
CPU1I				CPU1J			
BALLMAP_REV=1.4				BALLMAP_REV=1.4			
A17	VSS_001	VSS_091	AM27	AV11	VSS_181	VSS_271	G8
A23	VSS_002	VSS_092	AM3	AV14	VSS_182	VSS_272	H1
A26	VSS_003	VSS_093	AM36	AV17	VSS_183	VSS_273	H17
A35	VSS_004	VSS_094	AM37	AV3	VSS_184	VSS_274	H2
AA33	VSS_005	VSS_095	AM39	AV35	VSS_185	VSS_275	H23
AA34	VSS_006	VSS_096	AM38	AV38	VSS_186	VSS_276	H26
AA35	VSS_007	VSS_097	AM40	AV6	VSS_187	VSS_277	H29
AA36	VSS_008	VSS_098	AM44	AW10	VSS_188	VSS_278	H33
AA37	VSS_009	VSS_099	AM41	AW11	VSS_189	VSS_279	H35
AA38	VSS_010	VSS_100	AM5	AW16	VSS_190	VSS_280	H37
AA6	VSS_011	VSS_101	AN11	AW36	VSS_191	VSS_281	H39
AB5	VSS_012	VSS_102	AN14	AW6	VSS_192	VSS_282	H5
AC1	VSS_013	VSS_103	AN17	AY11	VSS_193	VSS_283	H6
AC6	VSS_014	VSS_104	AN19	AY14	VSS_194	VSS_284	H11
AD33	VSS_015	VSS_105	AN22	AY11	VSS_195	VSS_285	H9
AD36	VSS_016	VSS_106	AN24	AY35	VSS_196	VSS_286	J17
AD38	VSS_017	VSS_107	AN27	AY4	VSS_197	VSS_287	J20
AD39	VSS_018	VSS_108	AN30	AY6	VSS_198	VSS_288	J23
AD40	VSS_019	VSS_109	AN31	AY8	VSS_199	VSS_289	J26
AD5	VSS_020	VSS_110	AN32	B10	VSS_200	VSS_290	J29
AD6	VSS_021	VSS_111	AN33	B13	VSS_201	VSS_291	J32
AE3	VSS_022	VSS_112	AN34	B14	VSS_202	VSS_292	K1
AE33	VSS_023	VSS_113	AN35	B17	VSS_203	VSS_293	K12
AE36	VSS_024	VSS_114	AN36	B23	VSS_204	VSS_294	K13
AF1	VSS_025	VSS_115	AN5	B26	VSS_205	VSS_295	K14
AF34	VSS_026	VSS_116	AN6	B28	VSS_206	VSS_296	K17
AF36	VSS_027	VSS_117	AN7	B32	VSS_207	VSS_297	K2
AF37	VSS_028	VSS_118	AN8	B35	VSS_208	VSS_298	K20
AF40	VSS_029	VSS_119	AN9	B38	VSS_209	VSS_299	K23
AF5	VSS_030	VSS_120	AP1	B6	VSS_210	VSS_300	K26
AF6	VSS_031	VSS_121	AP11	C1	VSS_211	VSS_301	K29
AF7	VSS_032	VSS_122	AP17	C11	VSS_212	VSS_302	K33
AG36	VSS_033	VSS_123	AP17	C17	VSS_213	VSS_303	K35
AH2	VSS_034	VSS_124	AP22	C20	VSS_214	VSS_304	K37
AH3	VSS_035	VSS_125	AP25	C23	VSS_215	VSS_305	K39
AH33	VSS_036	VSS_126	AP27	C26	VSS_216	VSS_306	K5
AH36	VSS_037	VSS_127	AP30	C28	VSS_217	VSS_307	K6
AH37	VSS_038	VSS_128	AP36	C3	VSS_218	VSS_308	L10
AH38	VSS_039	VSS_129	AP37	C35	VSS_219	VSS_309	L17
AH39	VSS_040	VSS_130	AP4	C7	VSS_220	VSS_310	L20
AH40	VSS_041	VSS_131	AP40	C8	VSS_221	VSS_311	L23
AH45	VSS_042	VSS_132	AR11	D1	VSS_222	VSS_312	L26
AH8	VSS_043	VSS_133	AR14	D12	VSS_223	VSS_313	L29
AJ12	VSS_044	VSS_134	AR17	D20	VSS_224	VSS_314	L8
AJ15	VSS_045	VSS_135	AR18	D23	VSS_225	VSS_315	M1
AJ18	VSS_046	VSS_136	AR19	D26	VSS_226	VSS_316	M17
AJ21	VSS_047	VSS_137	AR27	D29	VSS_227	VSS_317	M2
AJ25	VSS_048	VSS_138	AR30	D32	VSS_228	VSS_318	M20
AJ27	VSS_049	VSS_139	AR36	D39	VSS_229	VSS_319	M23
AJ36	VSS_050	VSS_140	AR5	D39	VSS_230	VSS_320	M26
AJ5	VSS_051	VSS_141	AT1	D5	VSS_231	VSS_321	M29
AK1	VSS_052	VSS_142	AT11	D6	VSS_232	VSS_322	M33
AK10	VSS_053	VSS_143	AT10	D9	VSS_233	VSS_323	M35
AK13	VSS_054	VSS_144	AT12	E11	VSS_234	VSS_324	M37
AK14	VSS_055	VSS_145	AT13	E12	VSS_235	VSS_325	M39
AK16	VSS_056	VSS_146	AT15	E17	VSS_236	VSS_326	M5
AK22	VSS_057	VSS_147	AT16	E20	VSS_237	VSS_327	M6
AK28	VSS_058	VSS_148	AT17	E23	VSS_238	VSS_328	M9
AK31	VSS_059	VSS_149	AT25	E26	VSS_239	VSS_329	M8
AK33	VSS_060	VSS_150	AT27	E32	VSS_240	VSS_330	M1
AK34	VSS_061	VSS_151	AT28	E36	VSS_241	VSS_331	P2
AK36	VSS_062	VSS_152	AT29	E7	VSS_242	VSS_332	P36
AK35	VSS_063	VSS_153	AT32	E8	VSS_243	VSS_333	P38
AK36	VSS_064	VSS_154	AT33	E10	VSS_244	VSS_334	P40
AK37	VSS_065	VSS_155	AT30	F1	VSS_245	VSS_335	P5
AK4	VSS_066	VSS_156	AT31	F10	VSS_246	VSS_336	P6
AK40	VSS_067	VSS_157	AT32	F13	VSS_247	VSS_337	R33
AK5	VSS_068	VSS_158	AT33	F14	VSS_248	VSS_338	R35
AK6	VSS_069	VSS_159	AT34	F17	VSS_249	VSS_339	R37
AK7	VSS_070	VSS_160	AT35	F2	VSS_250	VSS_340	R39
AK8	VSS_071	VSS_161	AT36	F20	VSS_251	VSS_341	R6
AK9	VSS_072	VSS_162	AT37	F23	VSS_252	VSS_342	T1
AL11	VSS_073	VSS_163	AT38	F26	VSS_253	VSS_343	T5
AL14	VSS_074	VSS_164	AT39	F29	VSS_254	VSS_344	T6
AL17	VSS_075	VSS_165	AT40	F35	VSS_255	VSS_345	U8
AL19	VSS_076	VSS_166	AT41	F37	VSS_256	VSS_346	V1
AL24	VSS_077	VSS_167	AT6	F39	VSS_257	VSS_347	V2
AL27	VSS_078	VSS_168	AT7	F5	VSS_258	VSS_348	V33
AL30	VSS_079	VSS_169	AT7	F6	VSS_259	VSS_349	V34
AL36	VSS_080	VSS_170	AT8	F9	VSS_260	VSS_350	V35
AL5	VSS_081	VSS_171	AT9	G11	VSS_261	VSS_351	V36
AM1	VSS_082	VSS_172	AU1	G12	VSS_262	VSS_352	V37
AM11	VSS_083	VSS_173	AU15	G17	VSS_263	VSS_353	V38
AM14	VSS_084	VSS_174	AU26	G20	VSS_264	VSS_354	V39
AM17	VSS_085	VSS_175	AU34	G23	VSS_265	VSS_355	V40
AM2	VSS_086	VSS_176	AU36	G26	VSS_266	VSS_356	V5
AM21	VSS_087	VSS_177	AU6	G29	VSS_267	VSS_357	V6
AM23	VSS_088	VSS_178	AU8	G34	VSS_268	VSS_358	V5
AM25	VSS_089	VSS_179	AV10	G7	VSS_269	VSS_359	V8
AM25	VSS_090	VSS_180	AV10	G7	VSS_270	VSS_360	V8
A4	VSS_NCTF_01			AY37	VSS_NCTF_03		
AV39	VSS_NCTF_02	9 OF 10		B3	VSS_NCTF_04	10 OF 10	



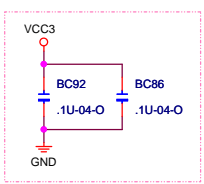
The processor memory controller does not have any DDR3 Data Mask (DM) signals for either channel. As a result the DM[8:0] pins of each DDR3 DIMM connector must be tied directly to ground.




For CHAD1



For CHAD2



PLACE BETWEEN CHA & CHB.  
DO NOT PUNCH VIA.

**Elitegroup Computer Systems**

Title

DDR3 - CHA DIMM0/1

Size

Document Number

B75H2-AM-DNI

Custom

Rev

A

Date

Wednesday, February 01, 2012

Sheet

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of

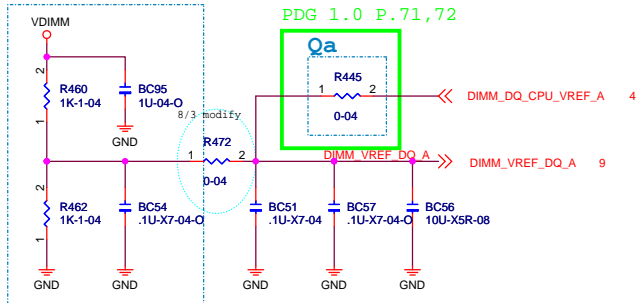
46





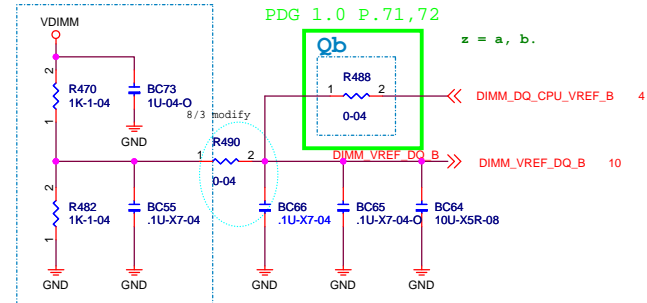


Pa



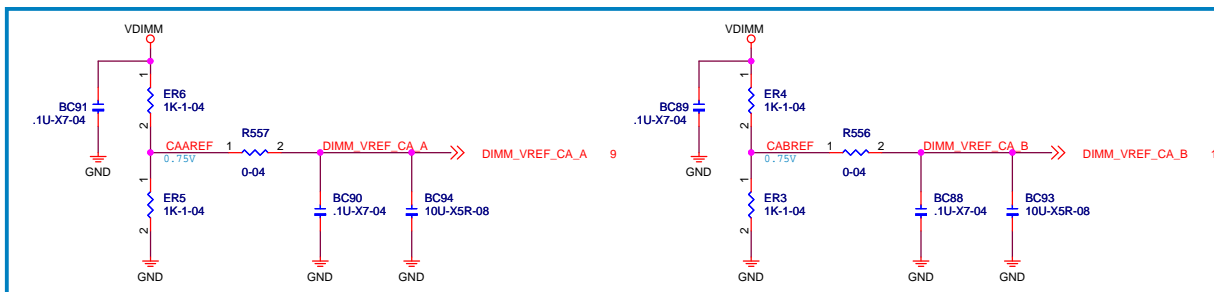
2011.08.25 Remove Divider Control Circuit

Pb



Layout Note:  
All parts close to DDR3 Slots.

DIMM\_VREF\_DQ Control Circuit



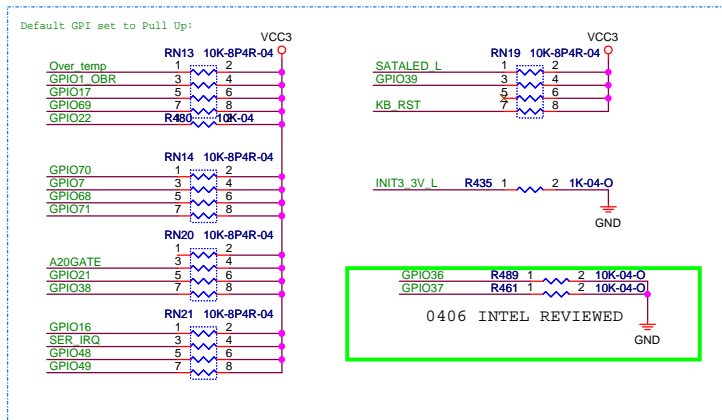
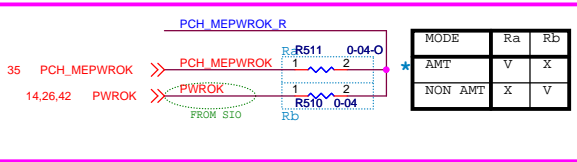
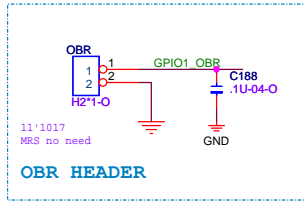
DIMM\_VREF\_CA Circuit



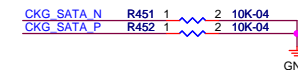




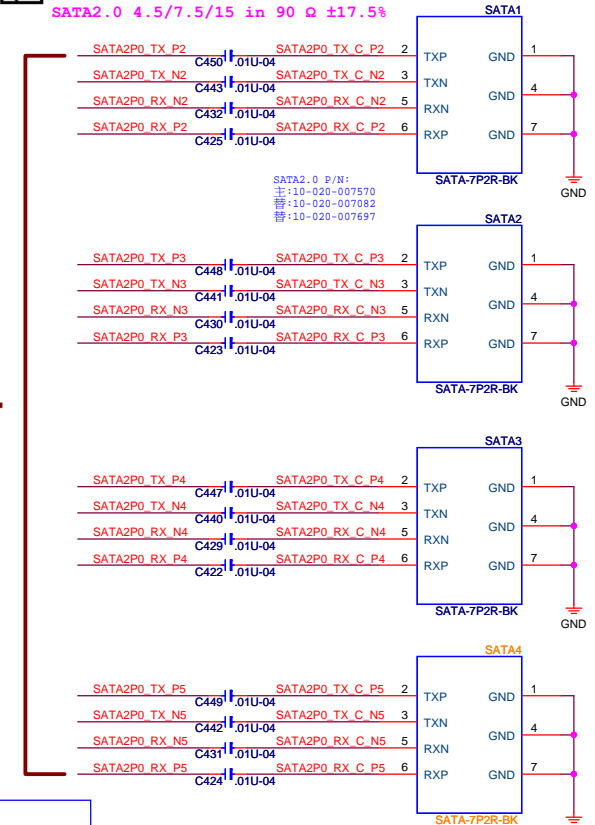
# DUAL NET MODE NO NEED SATA3.0



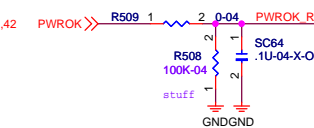
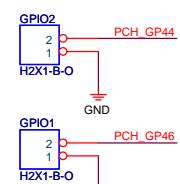
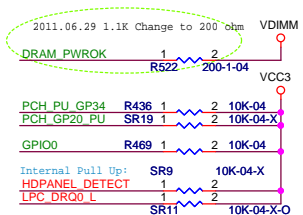
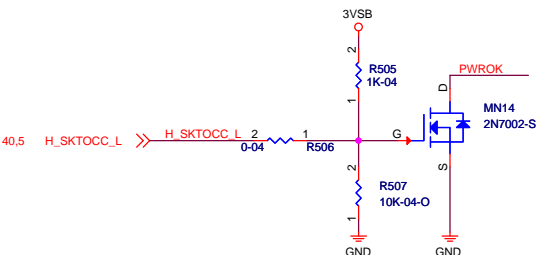
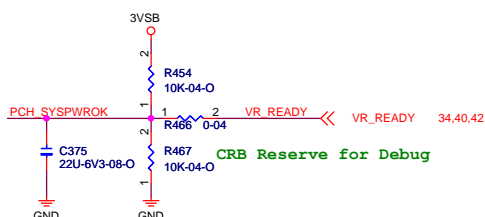
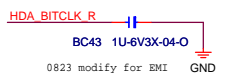
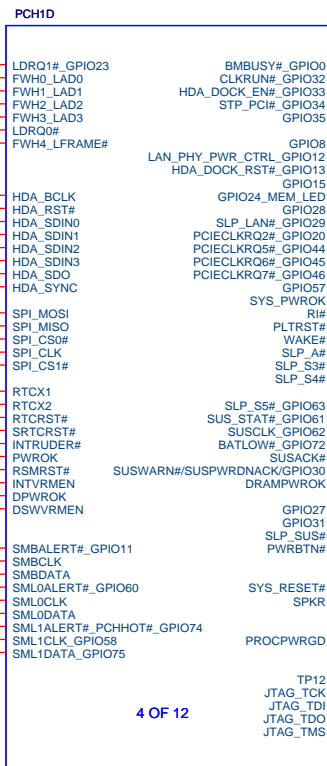
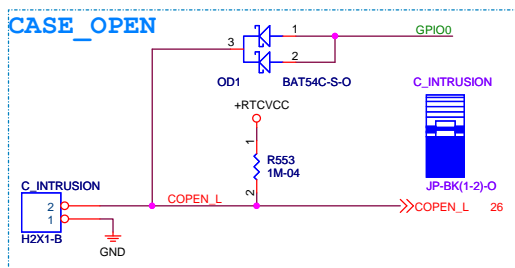
Stuff for Integrated Clock Mode



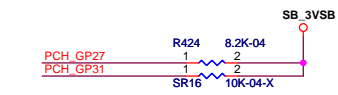
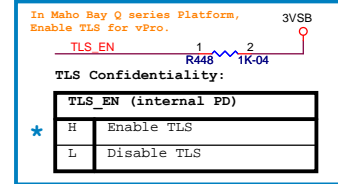
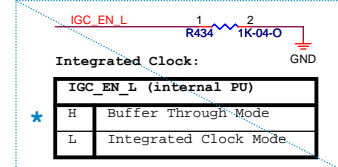
Layout Note:  
SATA3.0 4.5/7.5/20 in 90 Ω ±17.5%  
SATA2.0 4.5/7.5/15 in 90 Ω ±17.5%



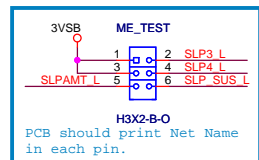
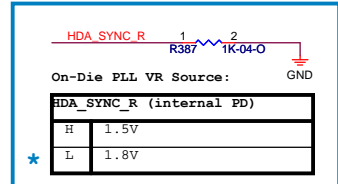
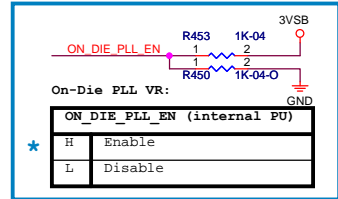
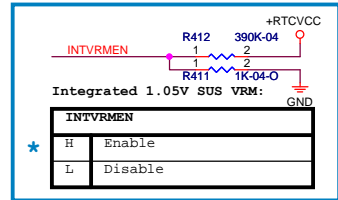
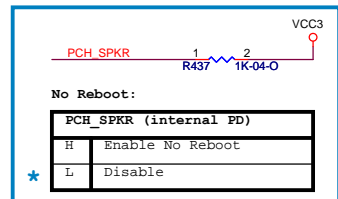
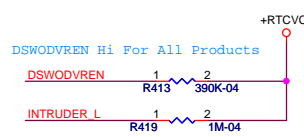
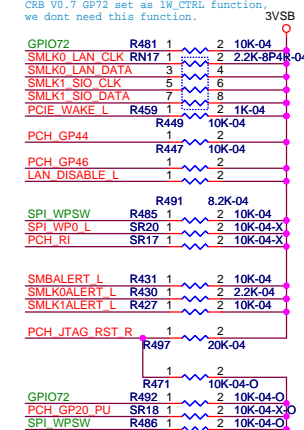




Buffer Through Mode /  
Integrated Clock Mode  
have been changed to F/W Strap.  
Default: Integrated Clock Mode  
Doc. Panther Point Platform Controller Hub  
(PCH) Family EDS Update V1.0

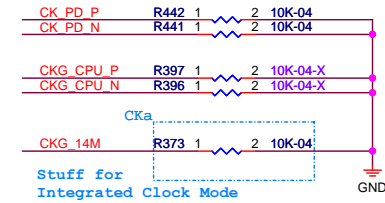
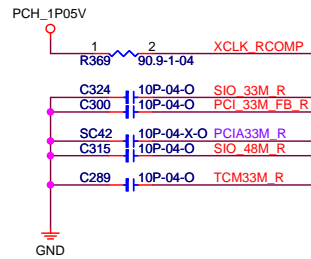


CRB V0.7 GP72 set as 1W\_CTRL function,  
we dont need this function. 3

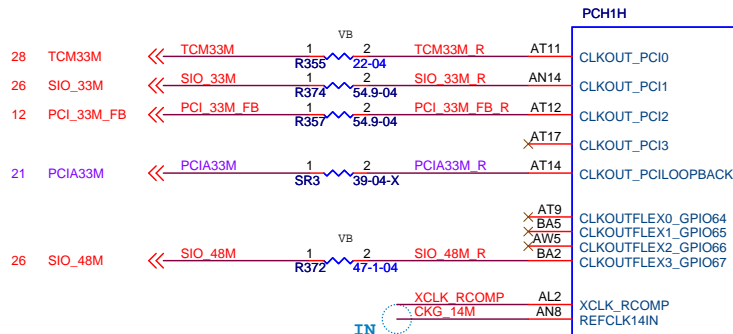


## ME Test Header

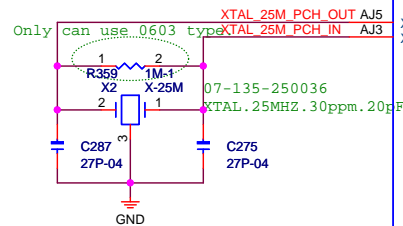




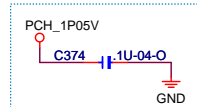
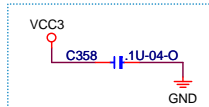
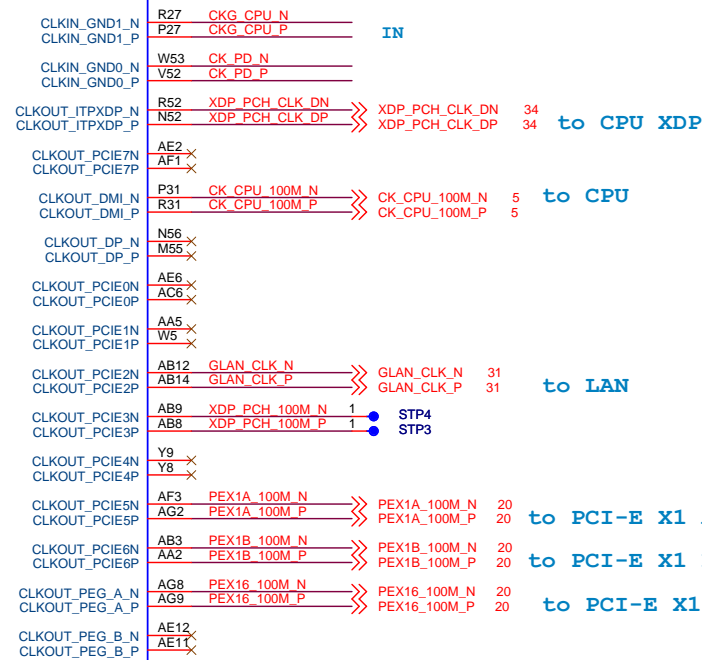
Clock Mode	CLK GEN. Seligo SLG421 Circuit.	CKa
Integrated Clock Mode	X	V
Buffer Through Mode	V	X



Layout Note:  
PCI Clock Max 15000MILS

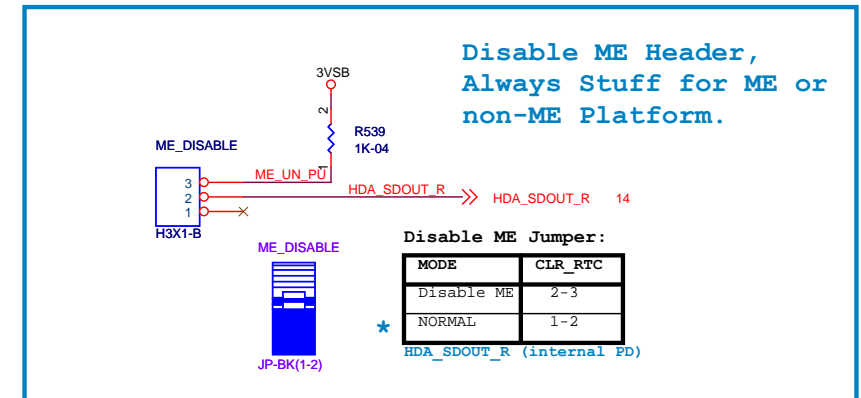
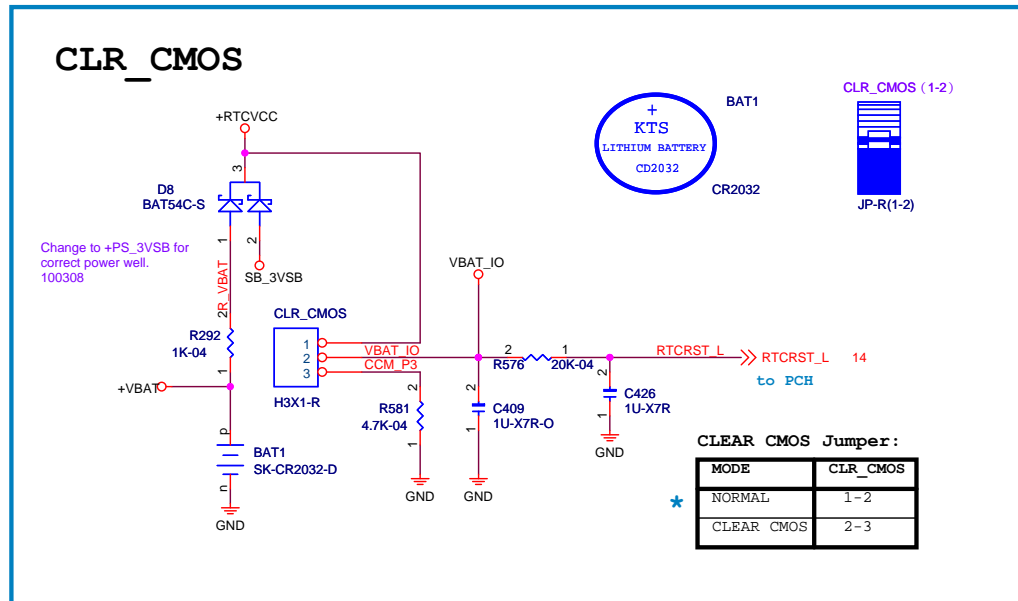
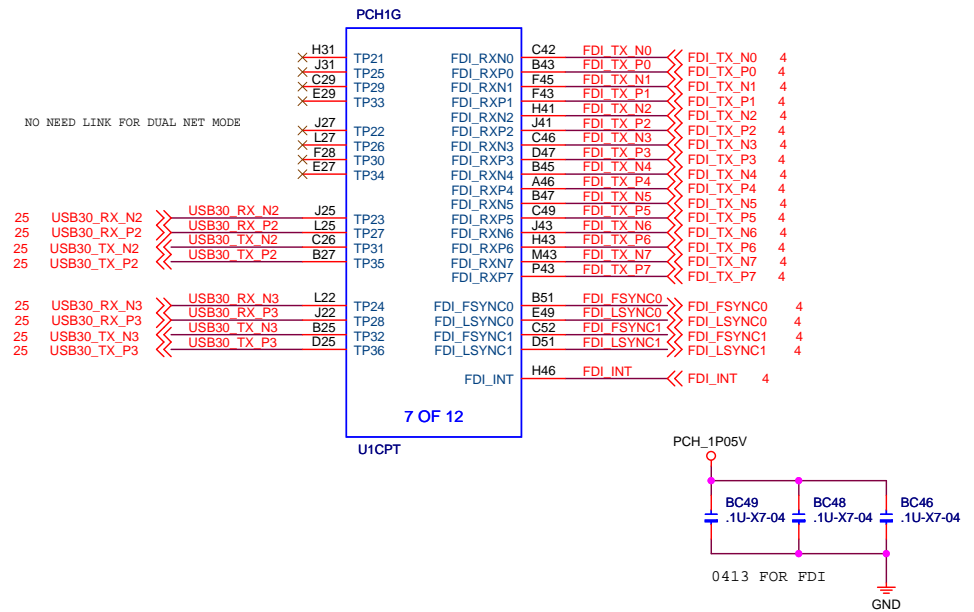
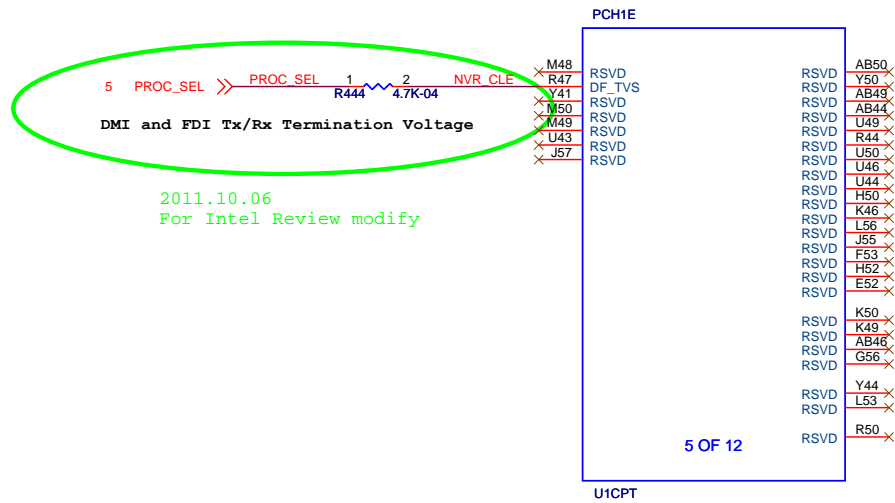


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Title			
PCH - CLK IO, CKG - SLG421			
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P	B75H2-AM-DNI	A	
Date:	Wednesday, February 01, 2012	Sheet	15 of 46

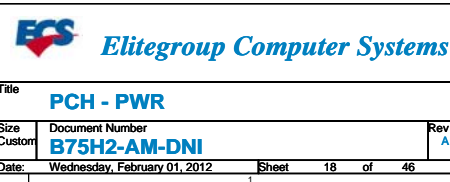




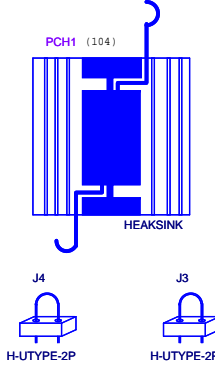
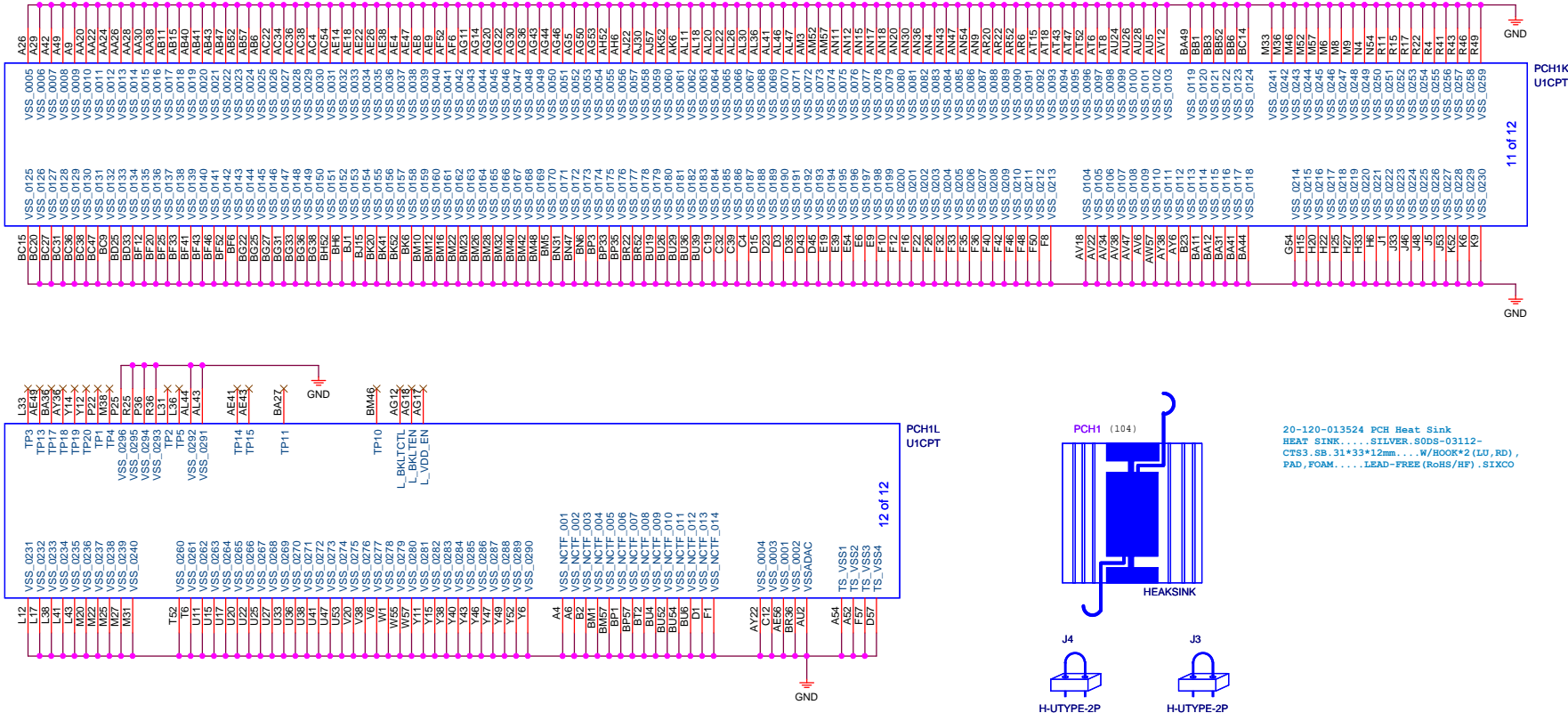












20-120-013524 PCH Heat Sink  
HEAT SINK.....SILVER.SODS-03112-  
CTS3.SB.31\*33\*12mm.....W/HOOK\*2 (LU, RD),  
PAD, FOAM.....LEAD-FREE (ROHS/HF) .SIXCO







PWRBTN\_L R  
OE\_L  
SEL1  
SLP3\_L

PWRBTN\_L R 20.29  
OE\_L 20.24,25,46  
SEL1 20.46  
SLP3\_L 14,20,24,25,26,35,36,38,42

## PCI V2.3

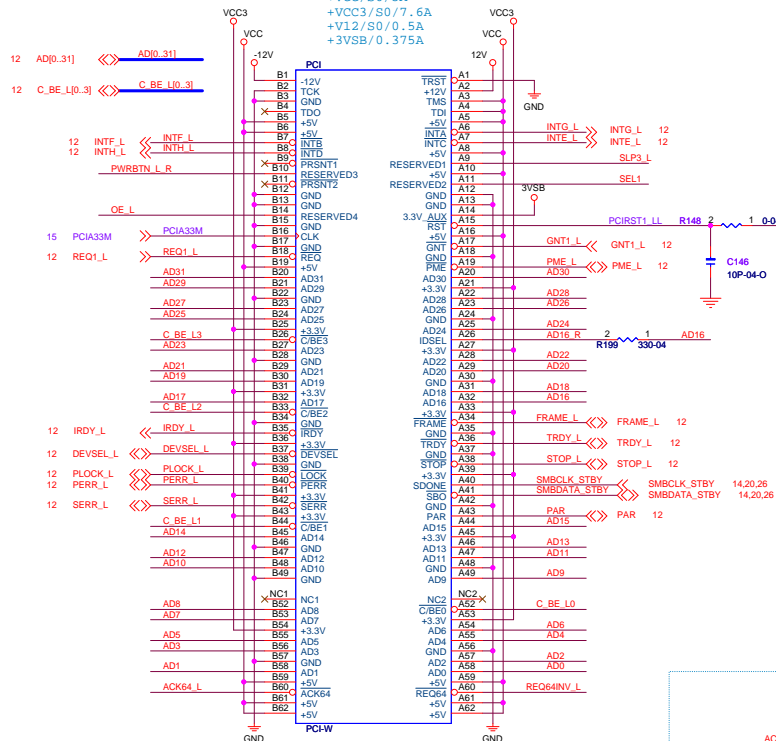
PCI Slot:

+VCC/S0/5A

+VCC3/S0/7.6A

+V12/S0/0.5A

+3VSB/0.375A



INT:G F E H

IDSEL:AD16

REQ/GNT:1

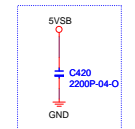
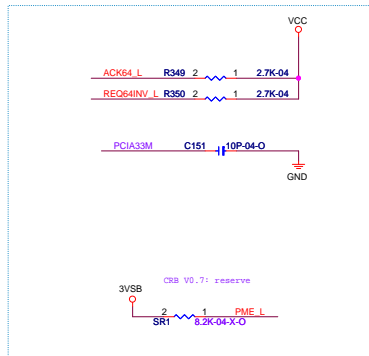
Follow CSB V0.7 Setup

## SEL1 from PCI/PCIE slot SEL#

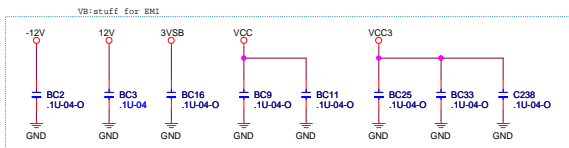
### DUAL-NET MODE CONTROL SIGNAL

PCI SLOT	PCIE1 SLOT	CONTROL SIGNAL
A9	A8	SLP_S3#
A11	A7	SEL#
B10	A5	PWRBTN#
B14	A6	OE#

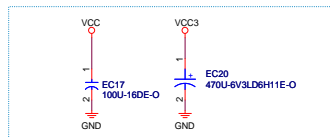
REMOVE PCI SOLT2



VB: add reserve for EMI AM stuff it



PCI1 Decoupling Cap.

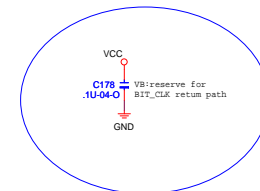
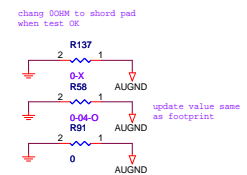
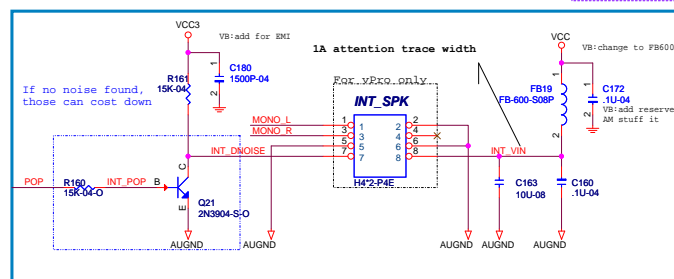
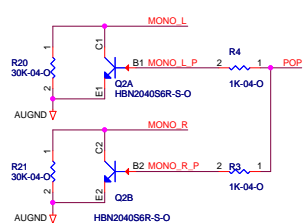
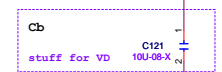
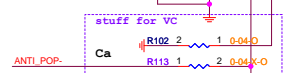
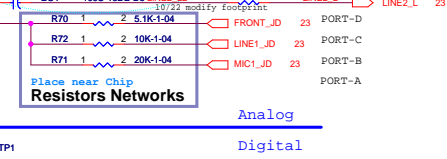
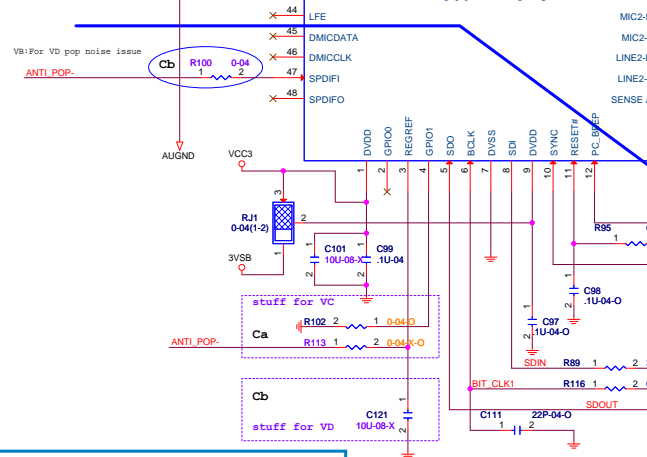
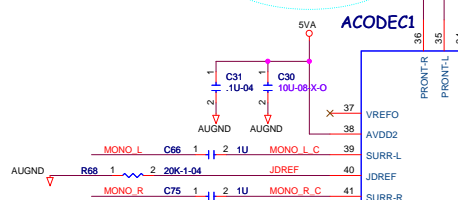
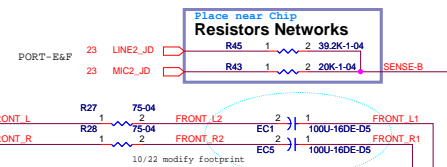
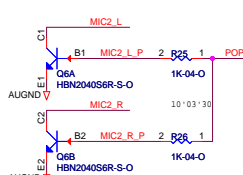
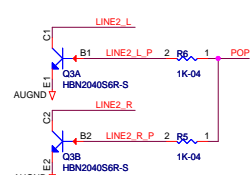
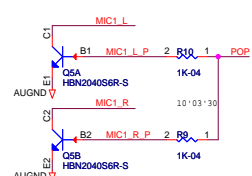
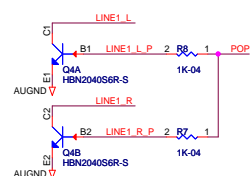
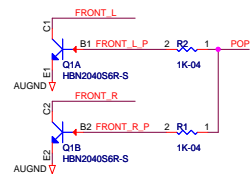
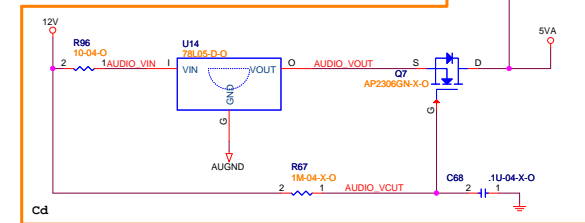
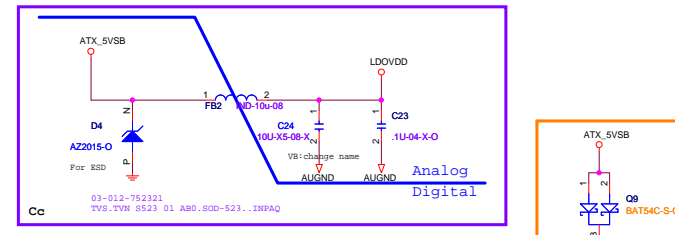


PCI1&PEX1B Decoupling Cap.



### Depop schematic

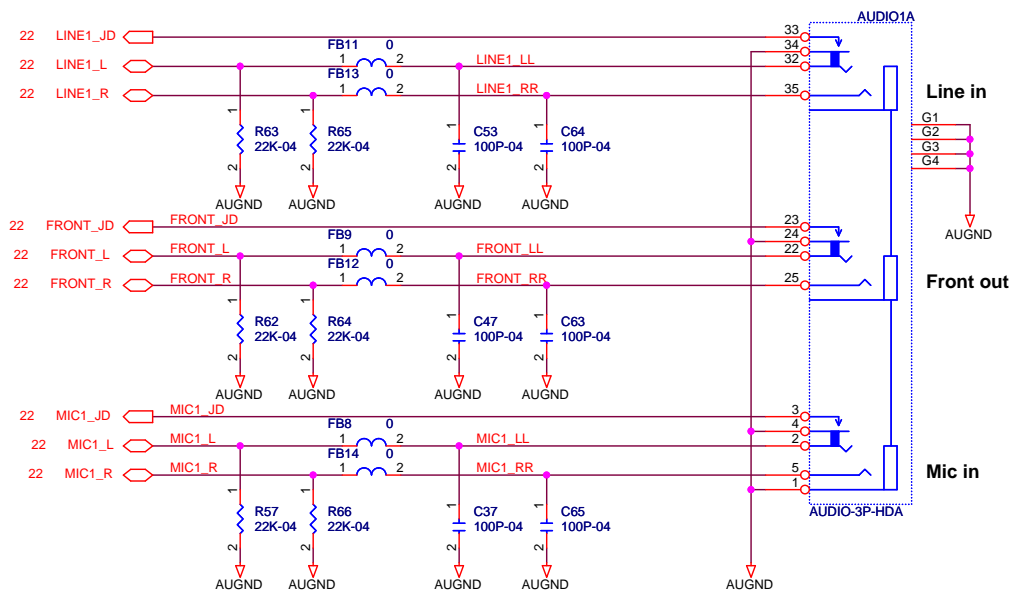
The schematic shows the internal structure of the MIC2754A-S voltage detector. It consists of two comparators, each with a non-inverting input (+) and an inverting input (-). The top comparator's non-inverting input is connected to the MIC2+VREF0 pin (pin 3), which is also connected to the R33 resistor. Its inverting input is connected to the MIC2-VREF0 pin (pin 1), which is also connected to the R31 resistor. The output of the top comparator is labeled MIC2\_R (pin 2) and has a pull-up resistor R36 connected to the MIC2+VREF0 pin. The bottom comparator's non-inverting input is connected to the MIC1-VREF0-L pin (pin 1), which is also connected to the R35 resistor. Its inverting input is connected to the MIC1\_VREF0-R pin (pin 2), which is also connected to the R35 resistor. The output of the bottom comparator is labeled MIC1\_L (pin 2) and has a pull-up resistor R35 connected to the MIC1-VREF0-L pin.



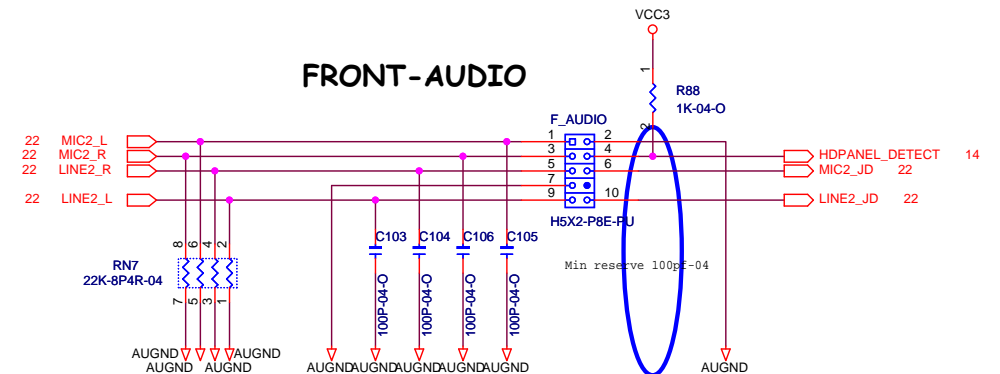
	ALC662 VC	ALC662 VD
Ca	V	X
Cb	X	V
Cc	X	V
Cd	V	X



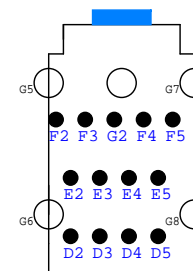
## REAR-AUDIO



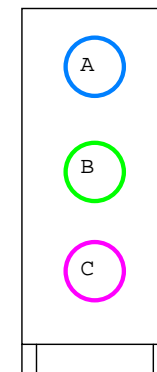
## FRONT-AUDIO



VB:remove SPDIF Circuit



TOP VIEW



FRONT VIEW

Line in

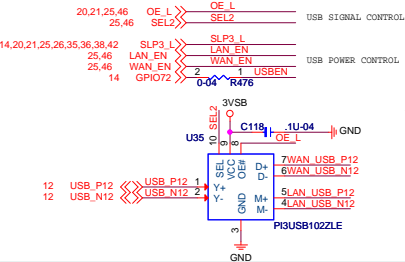
Line out

Mic in

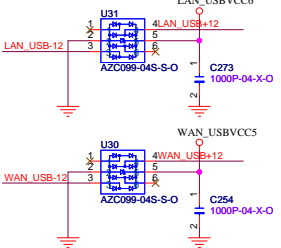
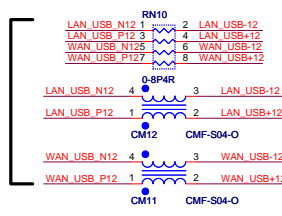
Title			
AUDIO ALC662 (PANEL)			
Size	Document Number		Rev
B	B75H2-AM-DNI		A
Date:	Wednesday, February 01, 2012		Sheet 23 of 46



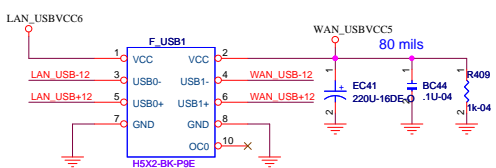
# FRONT PANEL USB HEADER



HDR 1



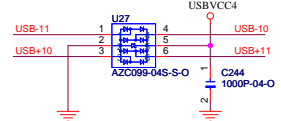
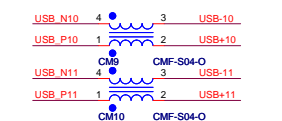
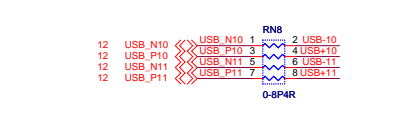
# FRONT PANEL USB HEADER 1



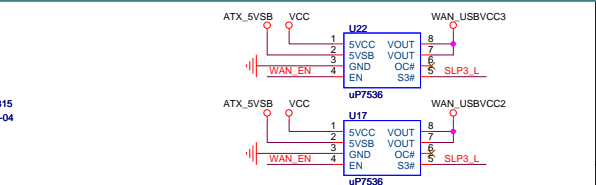
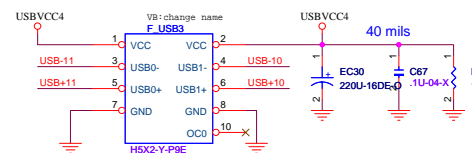
DNI Mode	ACPI State	S0/S3	S4	S5
SLP_S4#	SLP_S4# = H	SLP_S4# = L	SLP_S4# = L	SLP_S4# = L
Enable state	LAN_EN WAN_EN	LAN_EN WAN_EN	LAN_EN WAN_EN	LAN_EN WAN_EN
SEL1 =H SEL2=L	L H	L L	L L	L L
SEL1 =L SEL2=H	H L	L L	L L	L L
USB power state	Only one system USB power will be hold	Two systems USB power will be shut off	Two systems USB power will be shut off	Two systems USB power will be shut off
USB signal state	LAN link WAN link	NA	NA	NA
OE_L=0 enter DNI mode	L	L	L	L
OE_L=1 disable DNI mode	L	L	L	L

WAN/LAN USB is disable

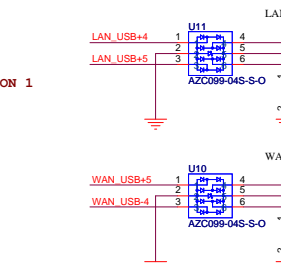
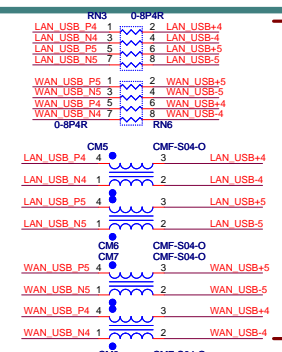
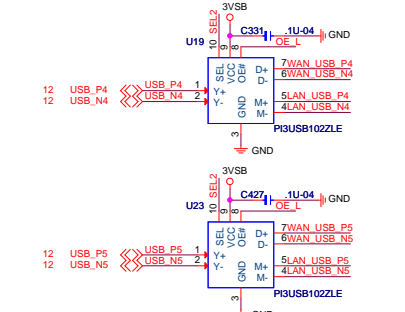
# HDR3 FOR DUAL NET MODE CARD



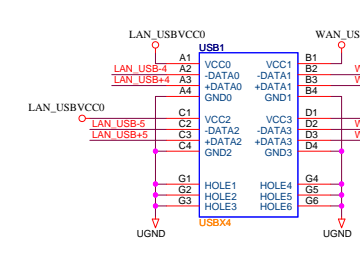
# 2ports for DUAL MODE Card



# REAR PANEL USB CONNECTOR

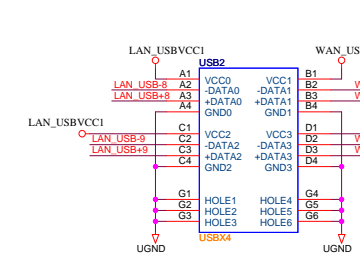


# REAR PANEL USB2.0 CONNECTOR 1

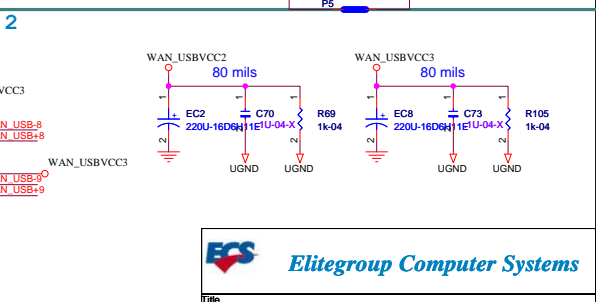
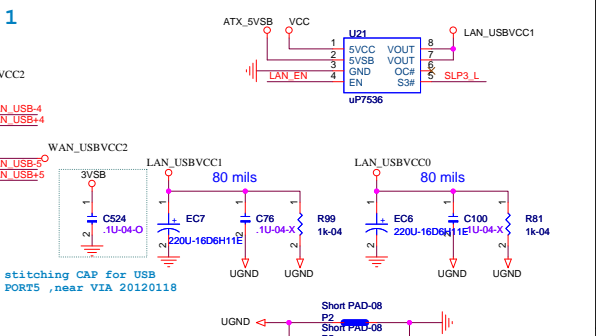


USB2.0\*4 Connector

# REAR PANEL USB2.0 CONNECTOR 2



USB2.0\*4 Connector



**DUAL NET MODE USB2.0 SW**

Document Number  
**B75H2-AM-DNI**

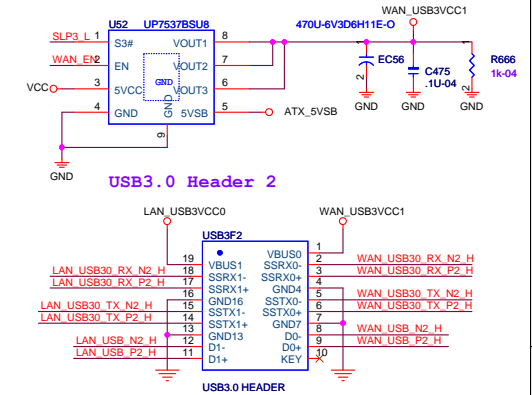
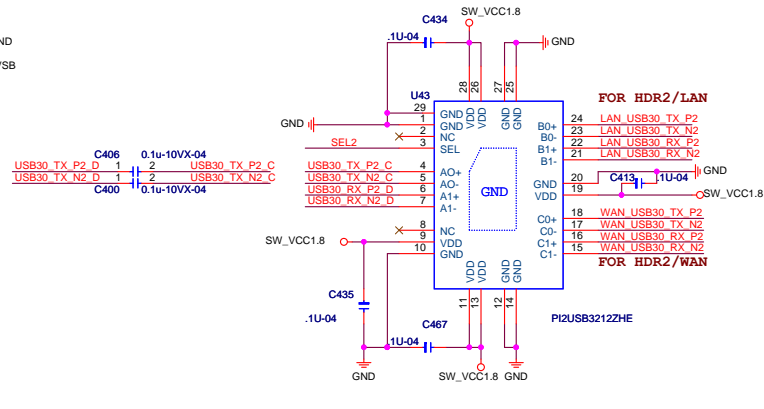
Date: Wednesday, February 01, 2012

Sheet 24 of 46

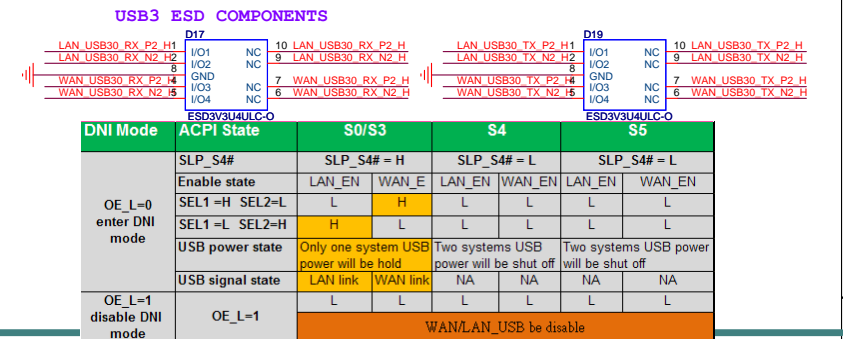
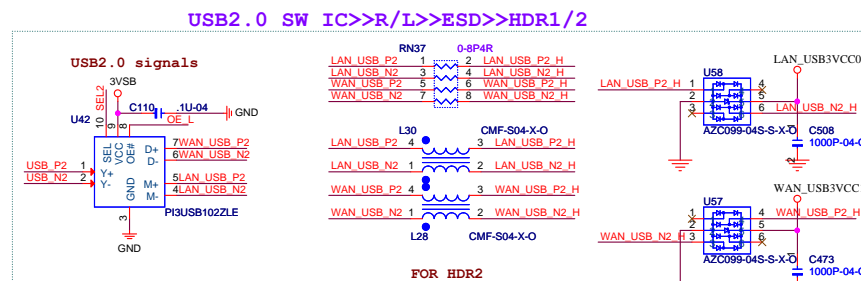
Rev A



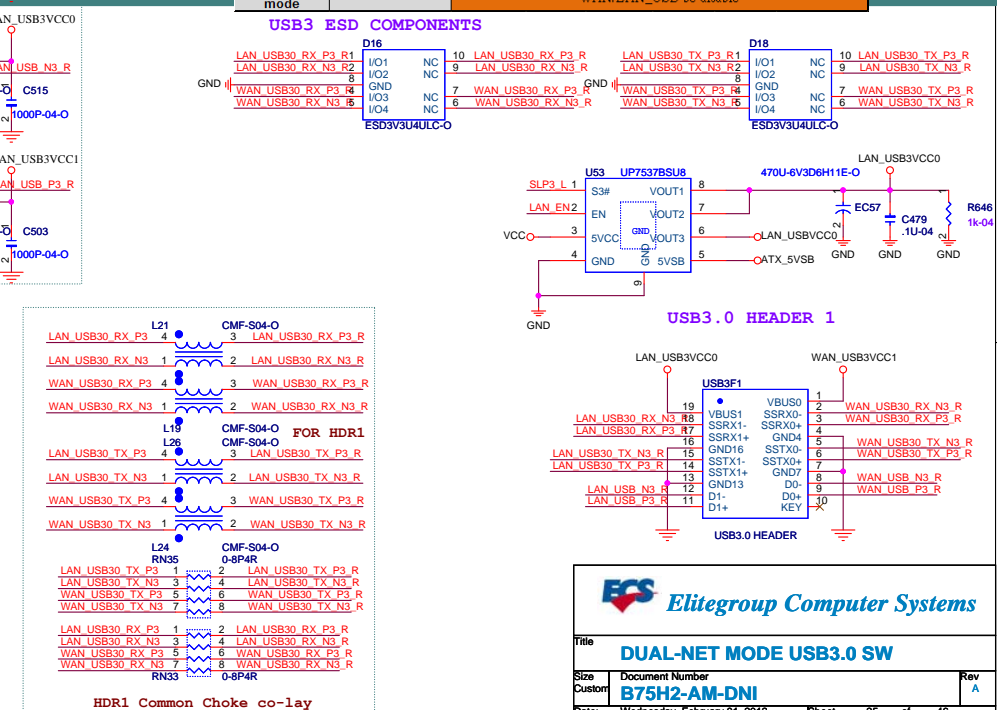
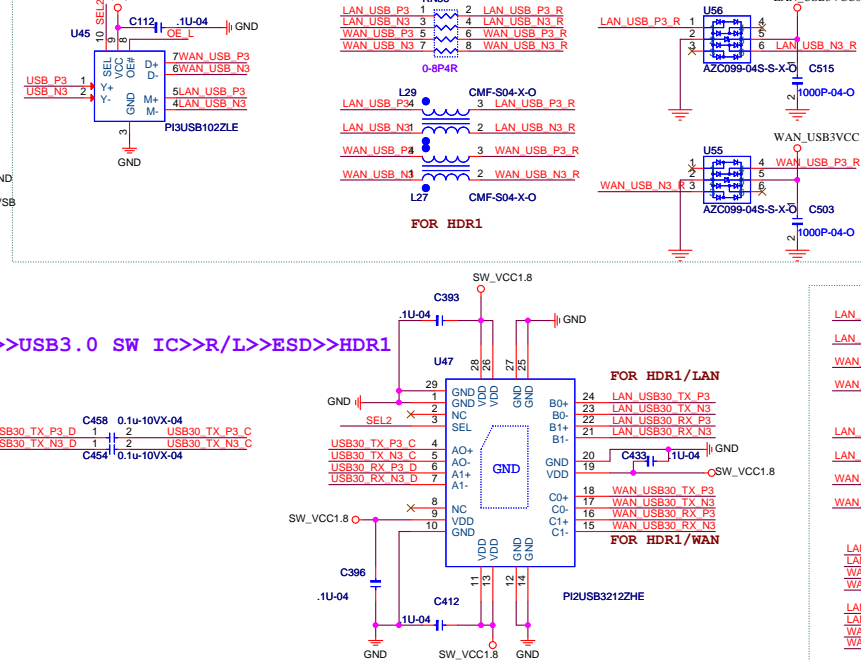
## RE-DRIVER&gt;&gt;USB3.0 SW IC&gt;&gt;R/L&gt;&gt;ESD&gt;&gt;HDR2



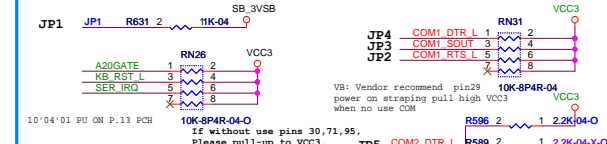
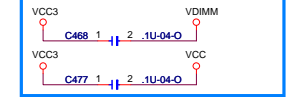
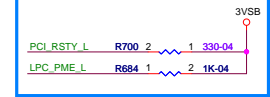
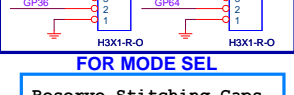
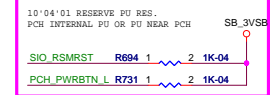
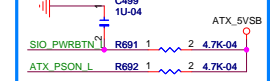
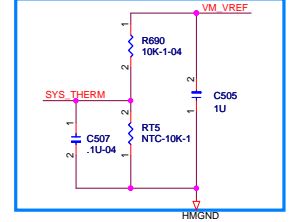
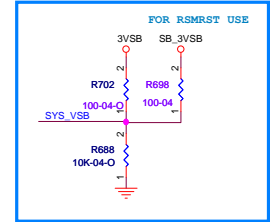
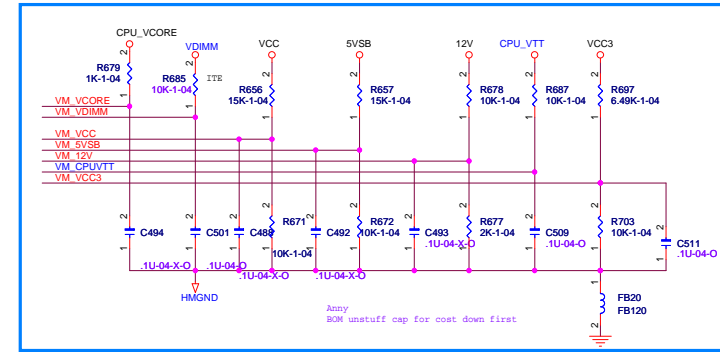
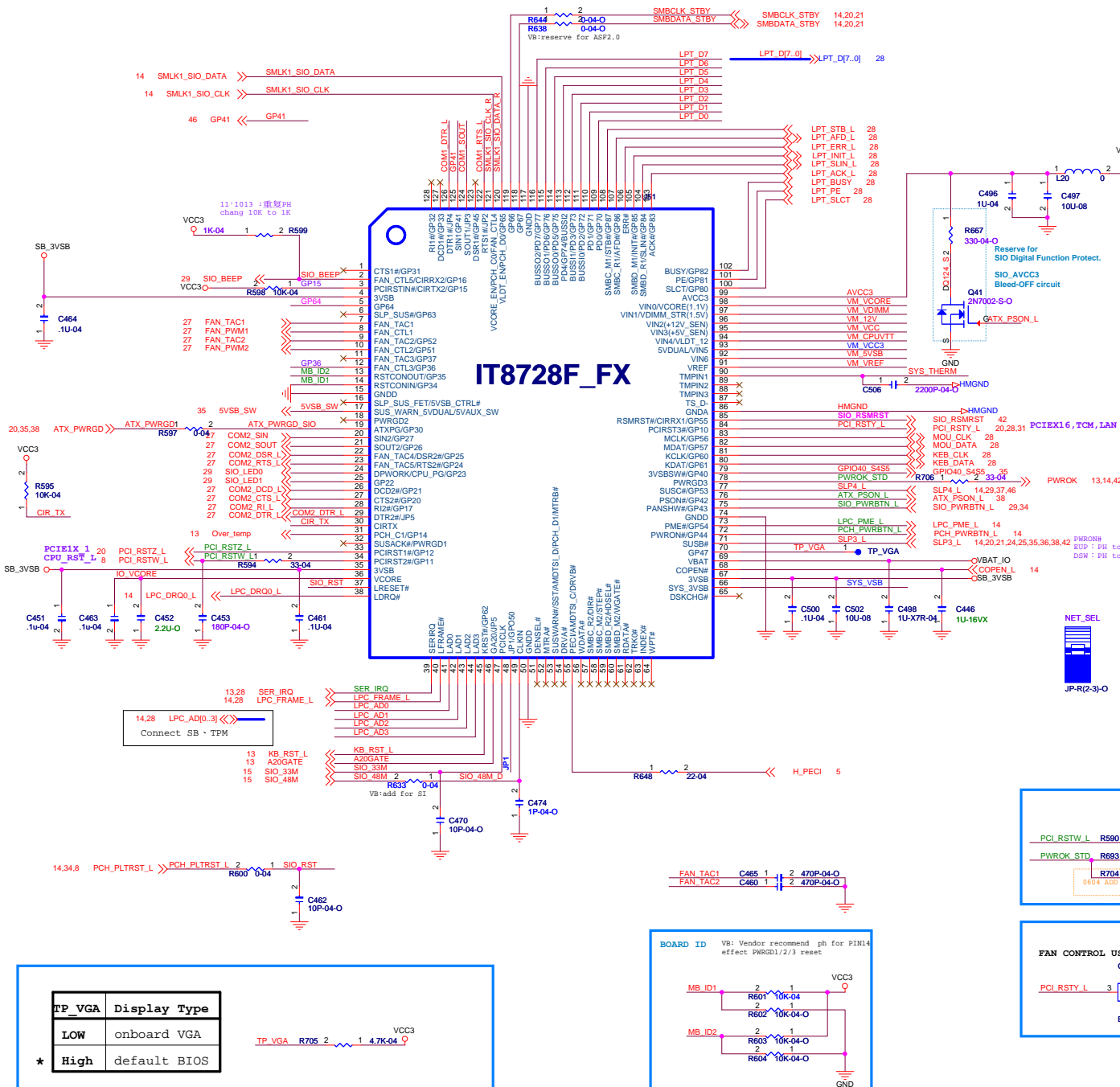
## USB2.0 SW IC&gt;&gt;R/L&gt;&gt;ESD&gt;&gt;HDR1/2



## RE-DRIVER&gt;&gt;USB3.0 SW IC&gt;&gt;R/L&gt;&gt;ESD&gt;&gt;HDR1

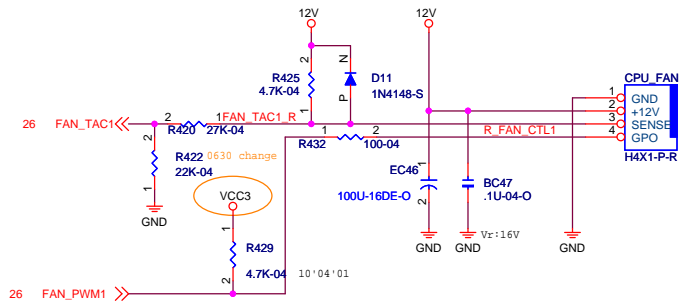






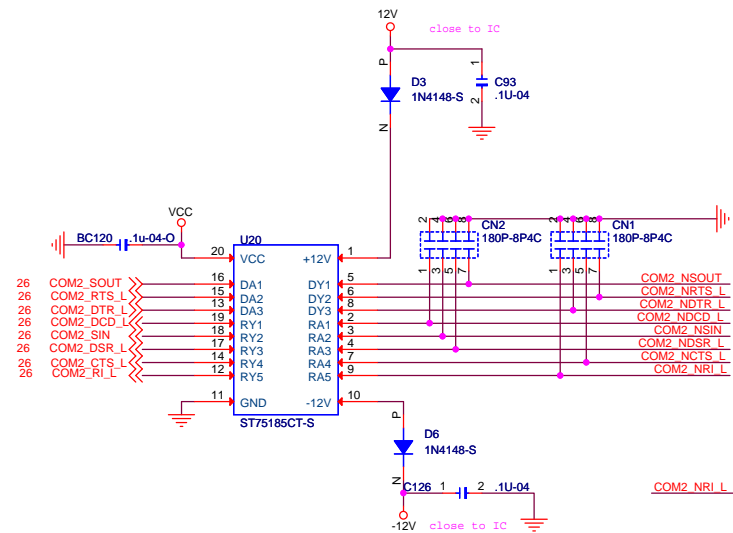
Strapping	Symbol	Value	Description	
JP1	DSW_EUP_SEL	1	EUP	*
Pin-48	DSW	0	DSW	
JP2	WDT_EN	1	Disable WDT to reset PWROK	*
Pin-122		0	Enable WDT to reset PWROK	
JP3	FAN_CTL_SEL	1	EC Index 63h/6Bh/73h is 80h	*
Pin-124		0	EC Index 63h/6Bh/73h is 00h	
JP4	K8PWR_EN	1	Disable K8 Power Sequence	*
Pin-126		0	Enable K8 Power Sequence	
JP5	UOVMODE_SEL	1	Notice Mode (Default)	*
Pin-29	OV/UV	0	Force Mode	



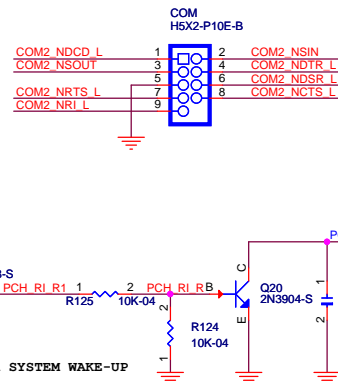


CPU FAN 4-PIN Circuit

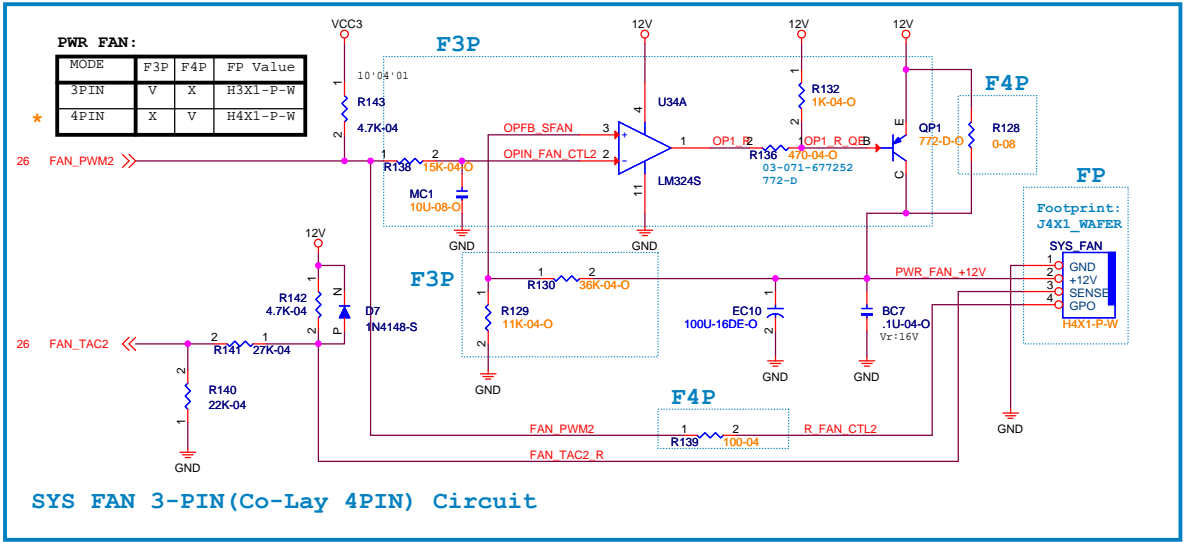
## COM PORT I/O



FOR SYSTEM WAKE-UP



COM PORT I/O

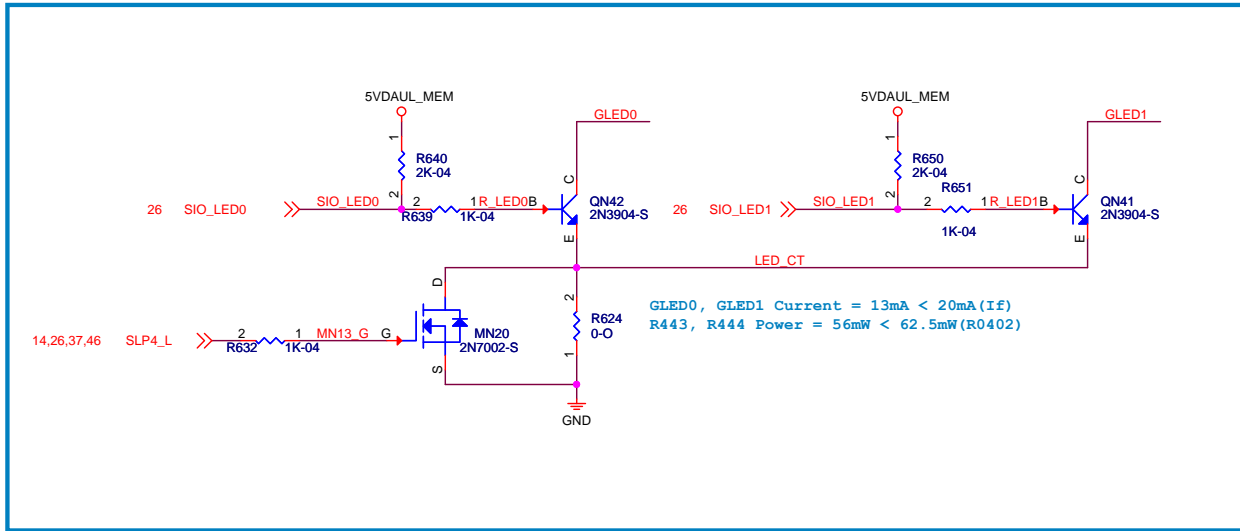
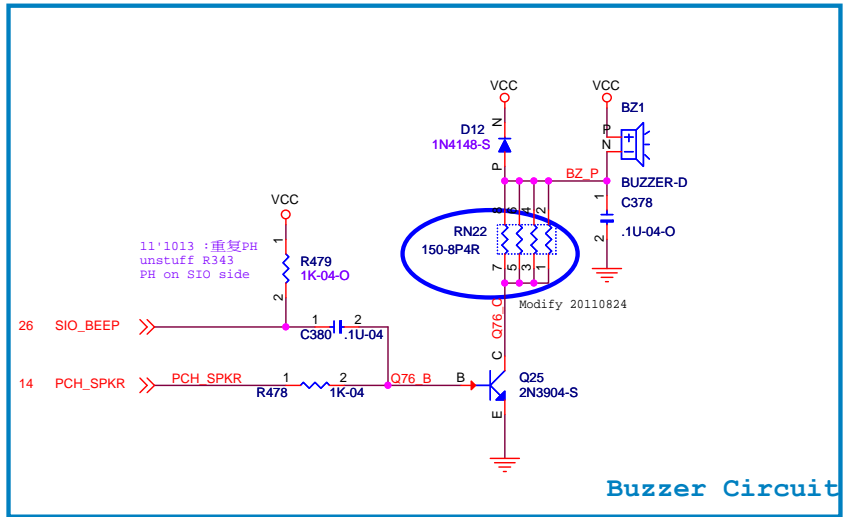
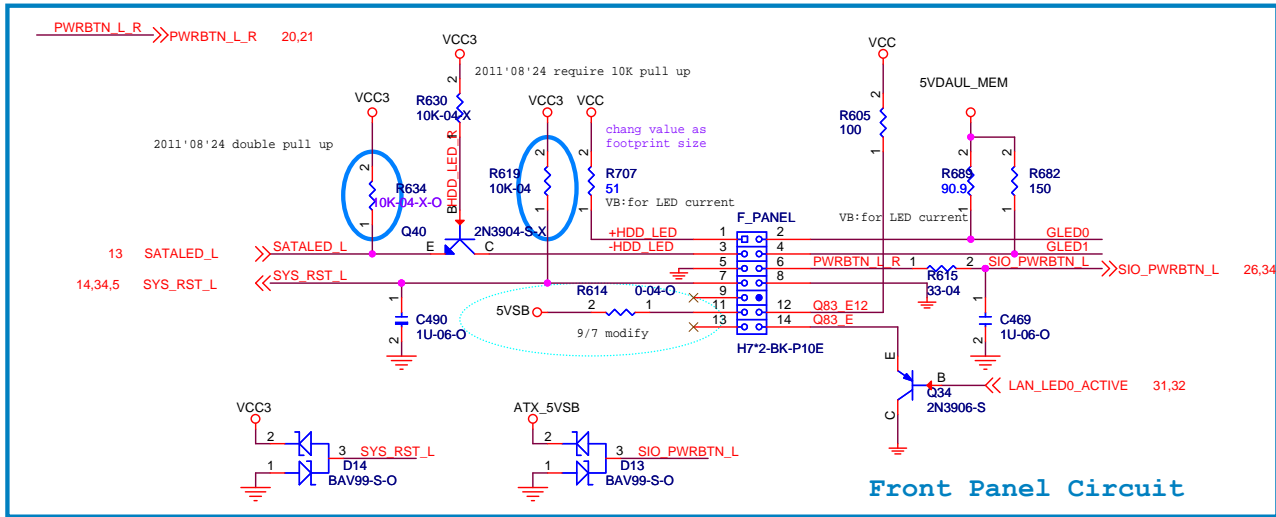


SYS FAN 3-PIN(Co-Lay 4PIN) Circuit







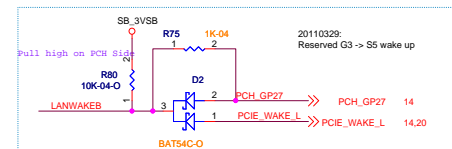
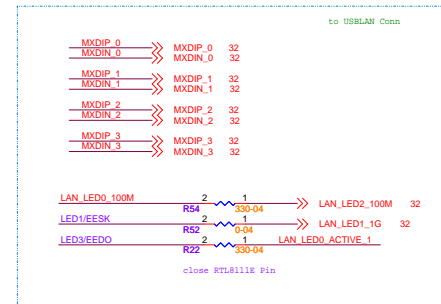
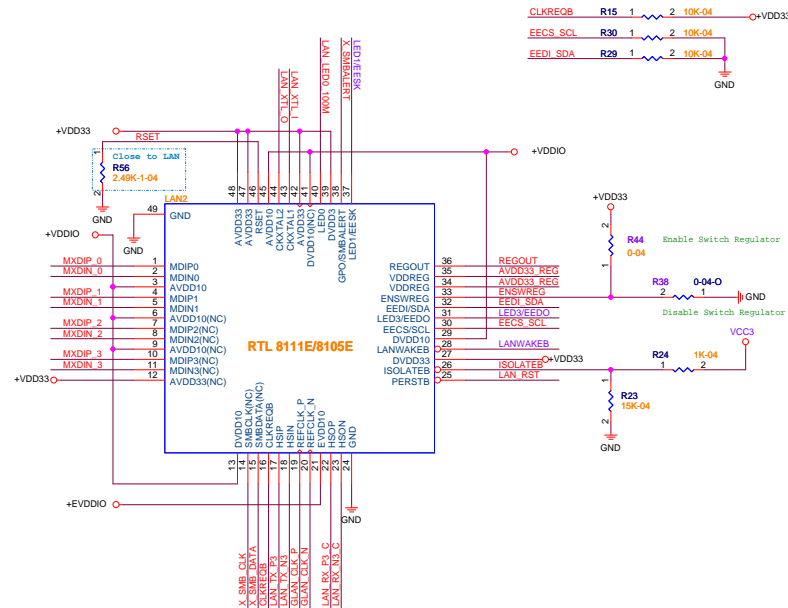
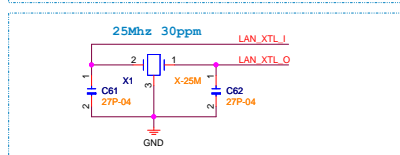
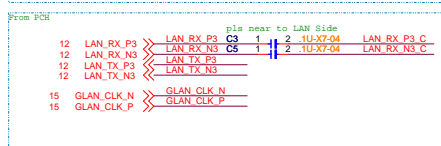
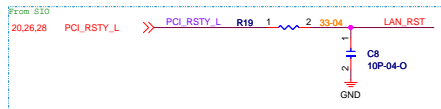


	LED	S0	S1	S3	S4/S5
Front Side	PWR LED (Single Color)	Always ON	Always ON	Blinking	OFF
	Storage LED (Single Color)	Access: Blink Others: OFF	Access: Blink Others: OFF	OFF	OFF
	LAN LED (ACTIVE) (Single Color)	Access: Blink Others: OFF	Access: Blink Others: OFF	OFF	OFF



REMOVE INTEL LAN FOR DUAL NET MODE





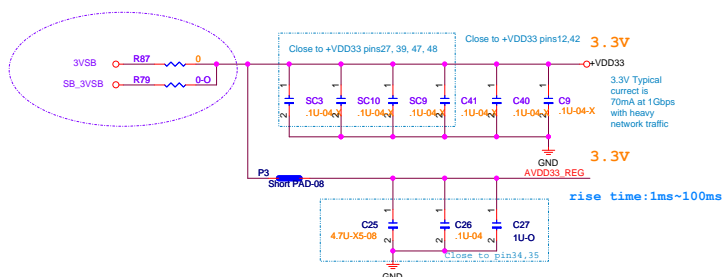
# The power inductor SPEC.

L(sat)/ tolerance	ESR(ohm) @ 1MHz	Max IDC (mA)	Efficiency
2.2 or 4.7 / <=20%	< 0.8	> 600	> 75 %

## Short Pad select

Value	Footprint	Width(min)	Current
Short PAD-04	20402-short-nmp	8mil	200mA
Short PAD-06	20603-short-nmp	12mil	300mA
Short PAD-08	20805-short-nmp	25mil	425mA
Short PAD-12	21209-short-nmp	30mil	950mA

Note: The Footprint add nmp is add SOLDER-MASK on the pad



BOM Different between RTL8111E,RTL8105E:  
For RTL8111E Series  
\*VDD10 pins-- 3, 6, 9, 13, 29, 41, 45.  
For RTL8105E-VB  
\* VDD10 pins-- 3, 13, 29, 45.  
For RTL8105E Series (except for VB)  
\* VDD10 pins-- 13, 29, 45.

BOM Different between RTL8111E,RTL8105E:  
For RTL8111E Series  
\*VDD33 pins-- 12, 27, 39, 42, 47, 48.  
For RTL8105E-VB  
\*VDD33 pins-- 27, 39, 42, 47, 48.  
For RTL8105E Series (except for VB)  
\*VDD33 pins-- 27, 39, 47, 48.

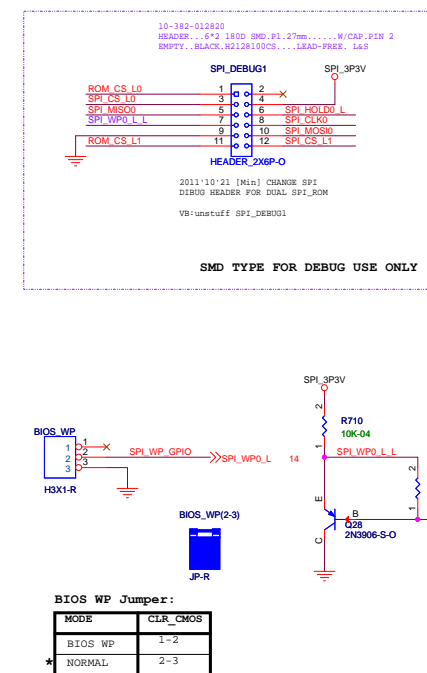
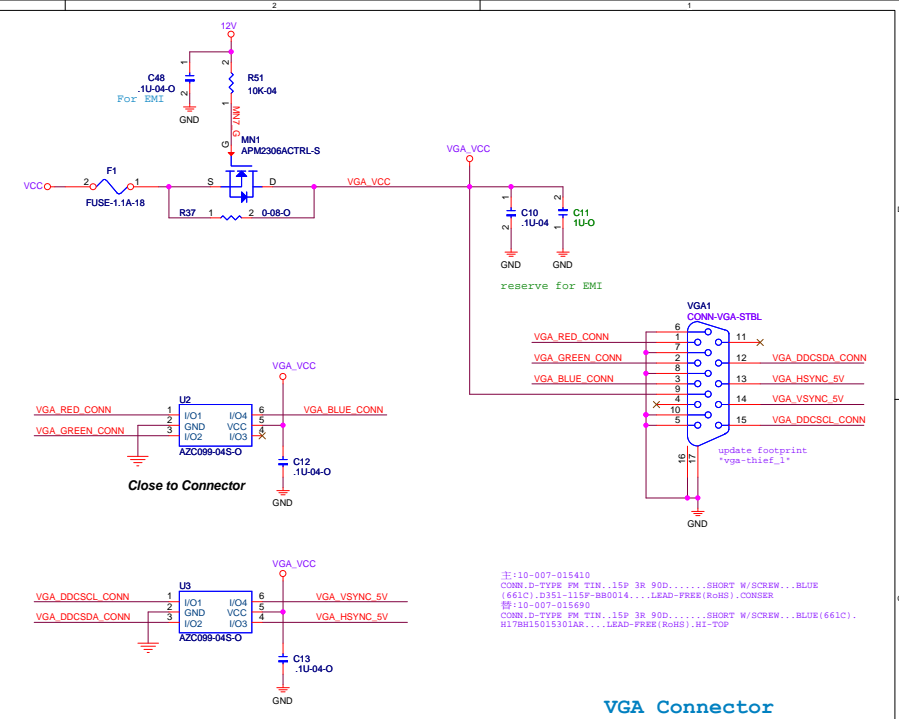
Acer/FDR request:  
1:default use e-FUSE;  
2:only reserve External EEPROM;  
3:B75 LAN使用 RTL8111E-VL-CG + 不用support ASF 2.0;









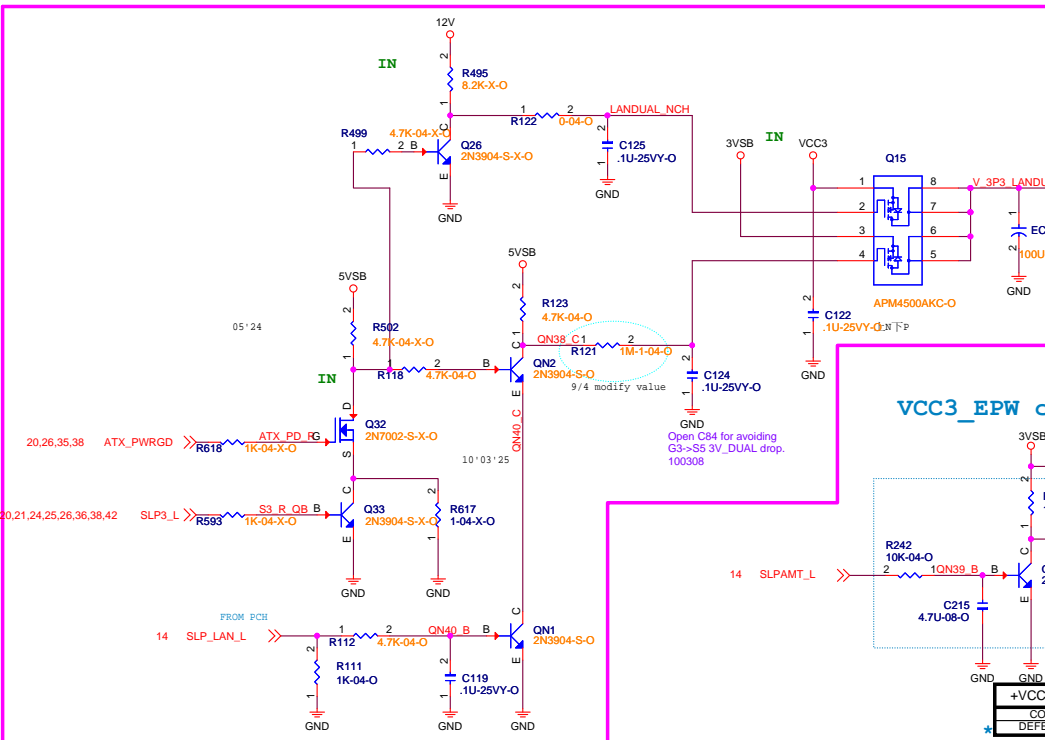








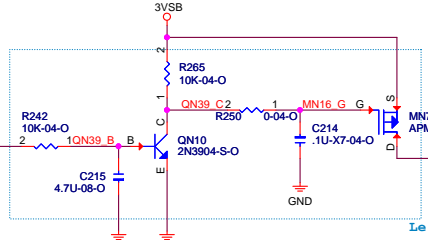
# for B75 DEL SCH



AMT 上件  
NON AMT 上件

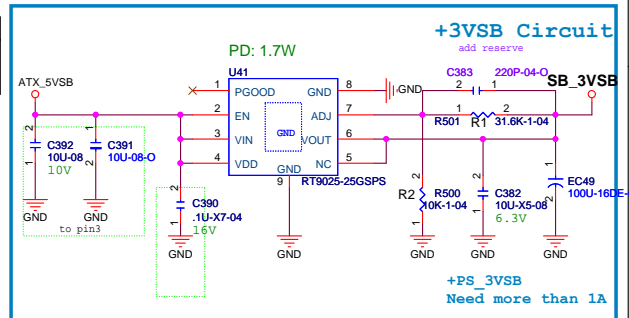
LAN Power Source	La	Lb	Lc
3V LANDUAL (Intel LAN)	V	X	X
Cost down (Intel LAN)	X	V	X
For Non-Intel LAN(NO WoL) or M0 Only	X	X	V

## VCC3\_EPW control

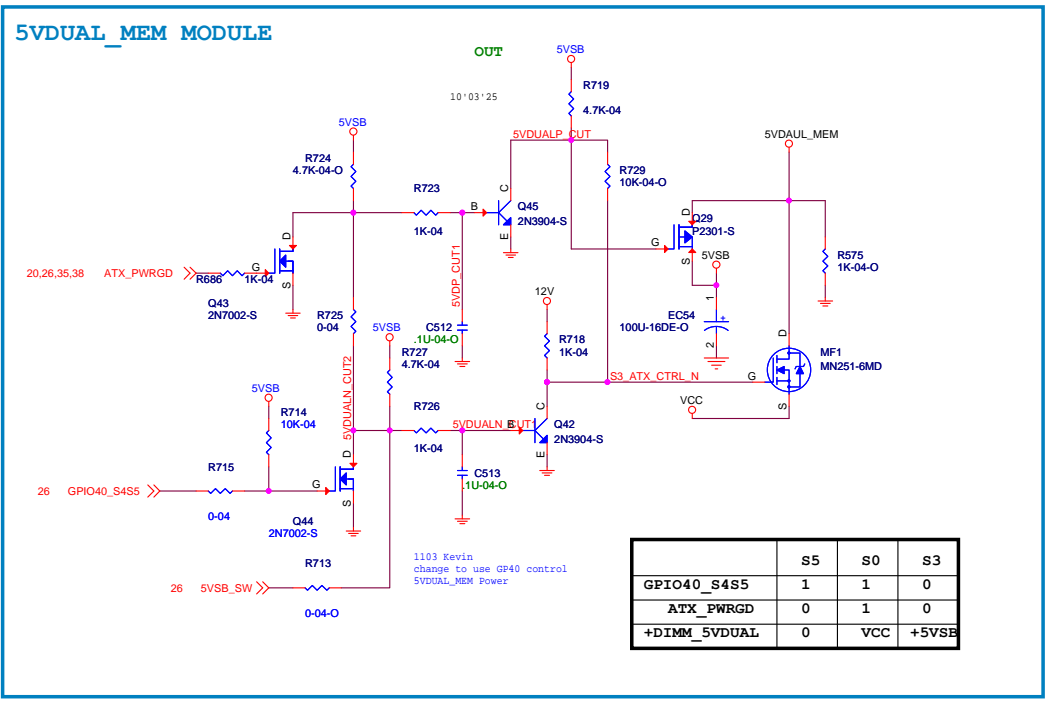


+VCC3_EPW	Ld	Le
COMBO	V	X
DEFENSIVE	X	V

R97 for Q77,B75

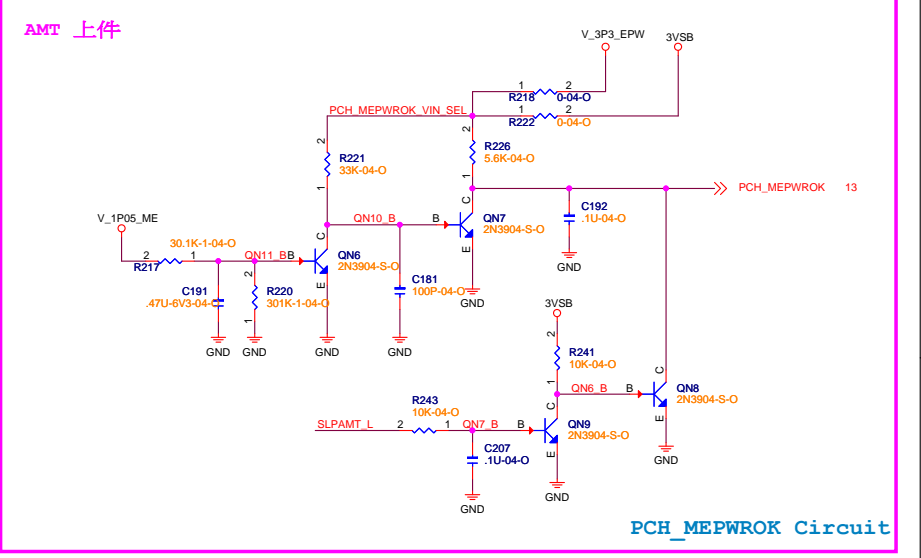


SR23 for H77



	S5	S0	S3
GPIO40_S4S5	1	1	0
ATX_PWRGD	0	1	0
+DIMM_5VDUAL	0	VCC	+5VSB

# for B75 DEL AMT SCH



**Elitegroup Computer Systems**

**Title** DC/DC 3VSB/3VDUAL/5VDUAL

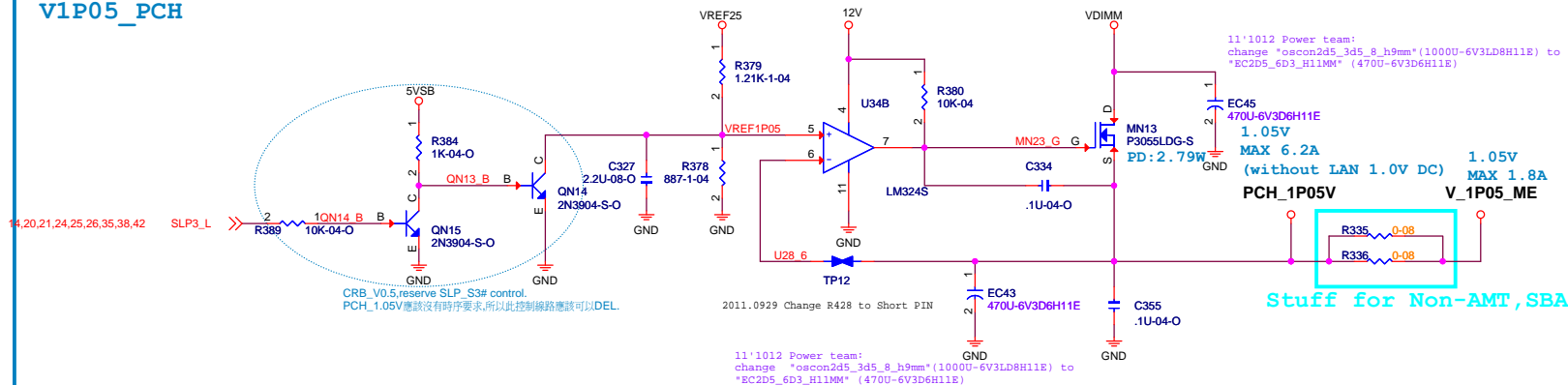
**Size** Custom    **Document Number** B75H2-AM-DNI    **Rev** A

**Date** Wednesday, February 01, 2012    **Sheet** 35 of 46



REMOVE ME POWER for Non-AMT,SBA

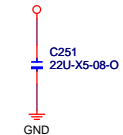
## V1P05\_PCH



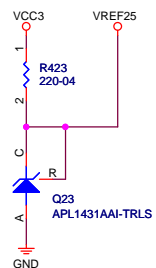
## BOM Note:

02-340-015840...\_dn10\_r8106a  
IC REG.RT8015AGQW.WDFN 10P.3A.LEAD-FREE(RoHS/HF).  
RICHTERK  
04-880-828100  
C/C.8.2pF.50V.0.25pf..NPO...SMD 0402....LEAD-FREE(RoHS/HF).  
05-152-240114  
RES.240K.1/16W.1%..SMD 0402.....LEAD-FREE(RoHS/HF).

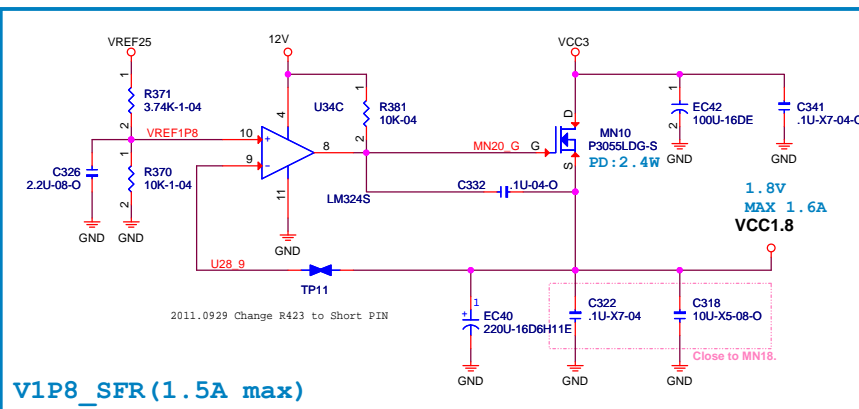
## V\_1P05\_ME



## VREF25



## V1P8\_SFR(1.5A max)





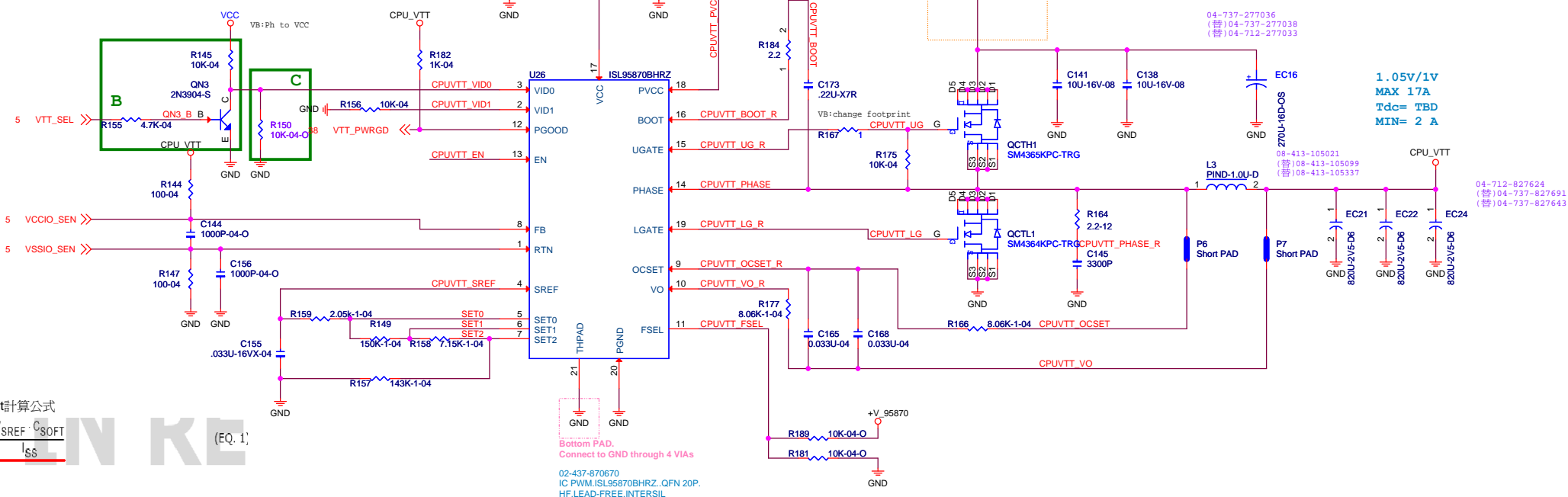
### BOM Different







VCCIO Voltage Selection		
	1.05V	1V
CPU(ES1 Sample)	Stuff B(control by VTT_SEL),unstuff C; Sandy=>VTT_SET=1	Stuff B(control by VTT_SEL),unstuff C; Ivy=>VTT_SET=0
CPU(ES2 Sample)	unstuff B and stuff C (for VTT_SEL 0)	X
CPU(QS)	1:unstuff B and stuff C; 2:Stuff B(control by VTT_SEL),unstuff C; Sandy/Ivy=>VTT_SET=1	C; X



Soft-start計算公式

$$t_{SS} = \frac{V_{SREF} \cdot C_{SOFT}}{I_{SS}} \quad (EQ. 1)$$

Where:

- $I_{SS}$  is the soft-start current source at the 20μA limit
- $V_{SREF}$  is the buffered  $V_{REF}$  reference voltage

Vout計算公式

TABLE 2. ISL95870B VID TRUTH TABLE

VID STATE		RESULT			
VID1	VID0	CLOSE	V <sub>SREF</sub>	V <sub>OUT</sub>	
1	1	SW0	V <sub>SET1</sub>	V <sub>OUT1</sub>	
1	0	SW1	V <sub>SET2</sub>	V <sub>OUT2</sub>	
0	1	SW2	V <sub>SET3</sub>	V <sub>OUT3</sub>	
0	0	SW3	V <sub>SET4</sub>	V <sub>OUT4</sub>	

Equations 21, 22, 23 and 24 give the specific  $V_{SET}$  equations for the ISL95870B setpoint reference voltages.

The ISL95870B  $V_{SET1}$  setpoint is written as Equation 21:  
 $V_{SET1} = V_{REF}$  (EQ. 21)

The ISL95870B  $V_{SET2}$  setpoint is written as Equation 22:  
 $V_{SET2} = V_{REF} \cdot \left(1 + \frac{R_{SET1}}{R_{SET2} + R_{SET3} + R_{SET4}}\right)$  (EQ. 22)

The ISL95870B  $V_{SET3}$  setpoint is written as Equation 23:  
 $V_{SET3} = V_{REF} \cdot \left(1 + \frac{R_{SET1} + R_{SET2}}{R_{SET3} + R_{SET4}}\right)$  (EQ. 23)

The ISL95870B  $V_{SET4}$  setpoint is written as Equation 24:  
 $V_{SET4} = V_{REF} \cdot \left(1 + \frac{R_{SET1} + R_{SET2} + R_{SET3}}{R_{SET4}}\right)$  (EQ. 24)

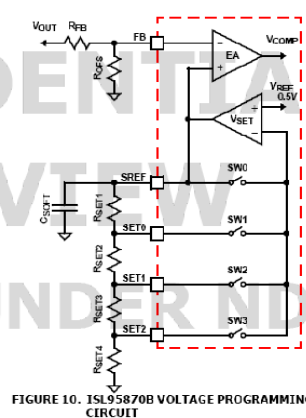
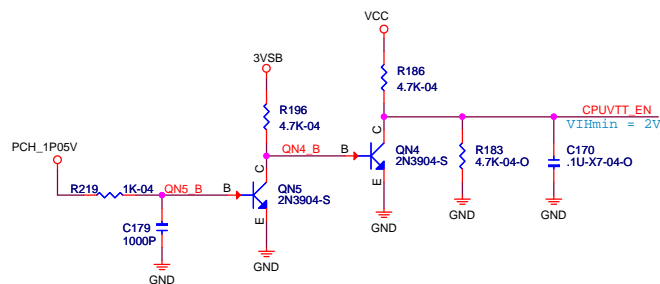


FIGURE 10. ISL95870B VOLTAGE PROGRAMMING CIRCUIT







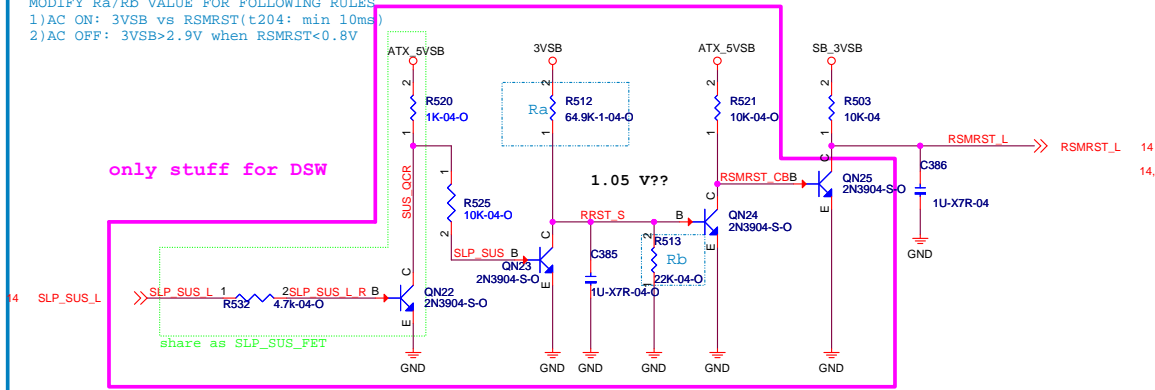




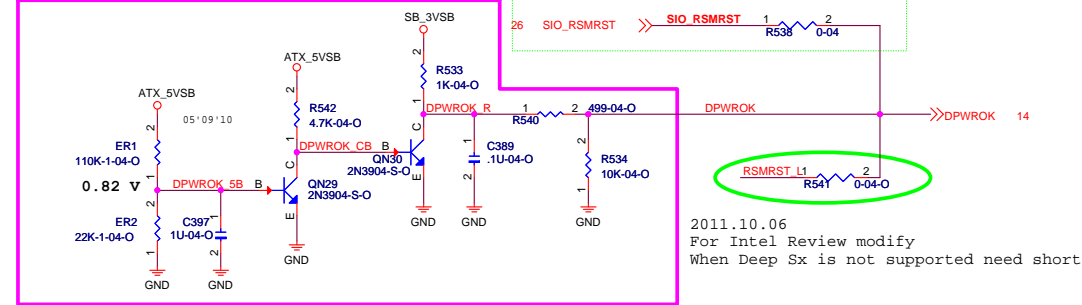


FOR DNI MODE DEL DSW 20120112

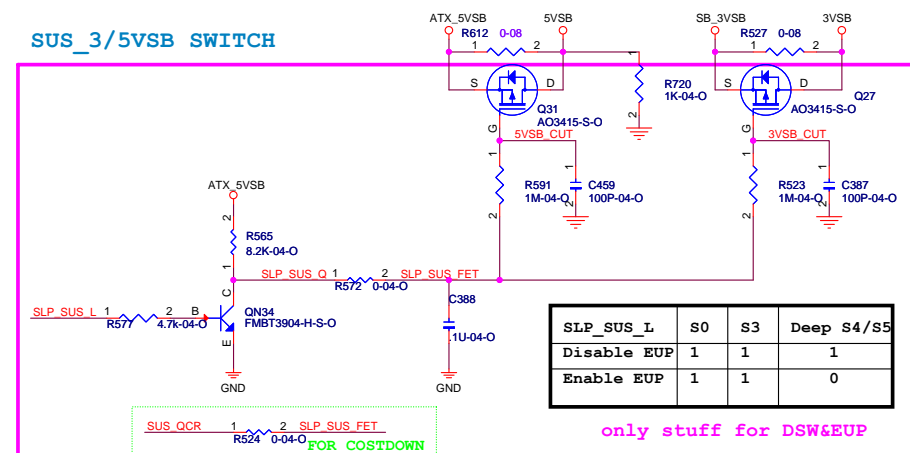
only stuff for DSW



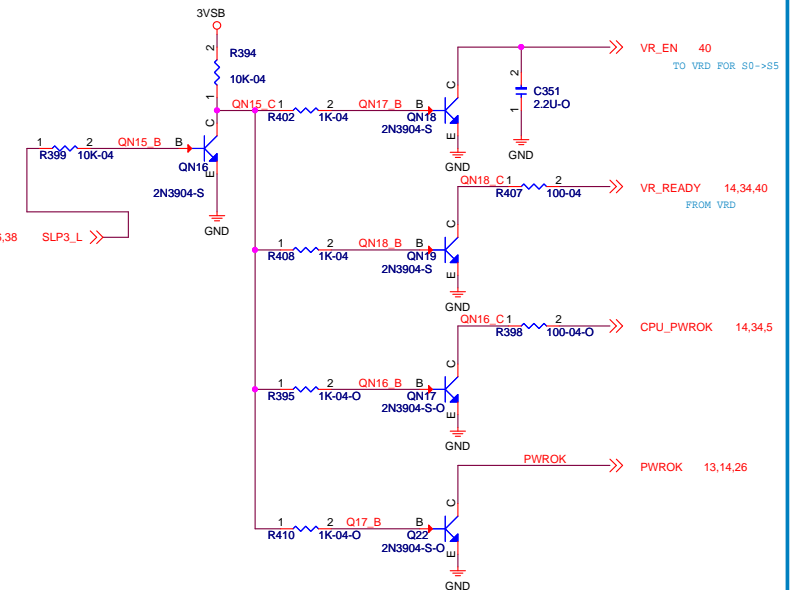
FOR COSTDOWN



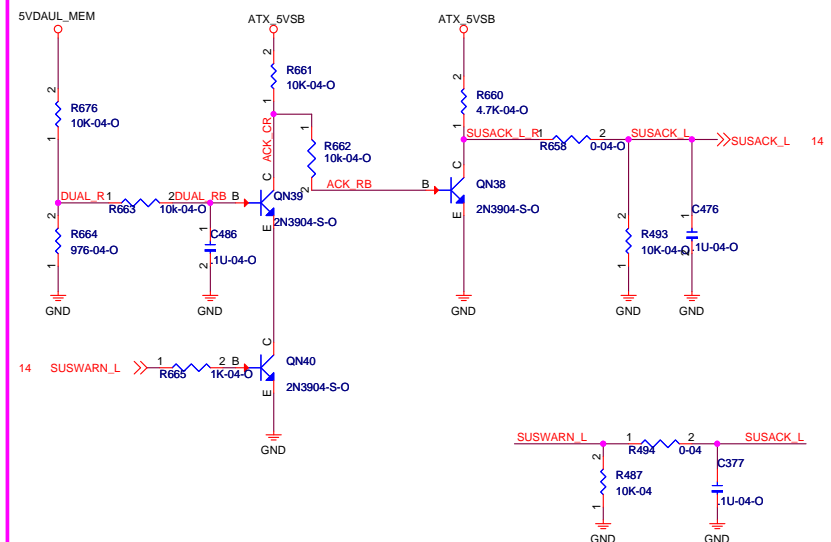
only stuff for DSW&EUP



SLP_SUS_L	S0	S3	Deep S4/S5
Disable EUP	1	1	1
Enable EUP	1	1	0



## SUSACK\_L CTRL CIRCUIT



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ATX P/S WITH 1A STBY CURRENT				
5VSB	5V	3.3V	12V	-12V
+/-5%	+/-5%	+/-5%	+/-5%	+/-5%

ATX4P
12V
+/-5%

Switching ISL6363 4+1 phases
------------------------------------

Switching ISL95870B 1 phase
-----------------------------------

Switching NCP1587
----------------------

DDR3 DIMM (2) 1333MHz	
VDDQ	15A_S0 1.0A_S3
V_SM_VTT	1.0A_S0

Linear LM324
-----------------

LDO APL5336
----------------

Linear LM324
-----------------

Intel Ivy Bridge CPU		
VCCP	V1D 0.25~1.52V	TDC :85A(95W)
VAXG	V1D 0.25~1.52V	25A
VTT	1.05V(1V)	8.5A
VCC_SA	0.925V(0.85V)	8.8A
VCCPLL	1.8V	1A
VDDQ	1.5V	4.75A

Intel Panther Point (TDP 5.5W)		
V_PROC_IO	1.05V	2mA
VccDMI	1.05V	0.057A
VccCORE	1.05V	2.52A
VccIO	1.05V	4.57A
VccADPLLA	1.05V	0.1A
VccADPLLB	1.05V	0.1A
VccCLKDMI	1.05V	0.08A
VccSSC	1.05V	0.105A
VccDIFFCLKN	1.05V	0.055A
VccASW(ME)	1.05V	1.61A
VccDFTERM	1.8V	0.2A
VccVRM	1.8V	0.185A
Vcc3_3	3.3V	0.409A
VccADAC	3.3V	0.068A
VccSPI	3.3V	0.02A
VccDSW3_3	3.3V	0.003A
VccSUS3_3	3.3V	0.1A
VccSUSHDA	3.3V	0.01A
VccRTC	3.3V	6uA(G3)
V5REF	5V	1mA
V5REF_SUS	5V	1mA

Fans
12V_200mA

SPI
VCC3_30mA

CRT
VCC_1A fuse

HDMI/DP
VCC3_0.5A fuse x1

HDMI L.S.
VCC3_180mA

Flash/NVM
VCC3_0.3A
1.8V_0.1A

Battery 3V
---------------

B75

REALTEK RTL8111E_VL		
VDD3P3	3.3V	70mA
VDD1P0	1.0V	300mA
CTRL1P0 internal LVR Output		

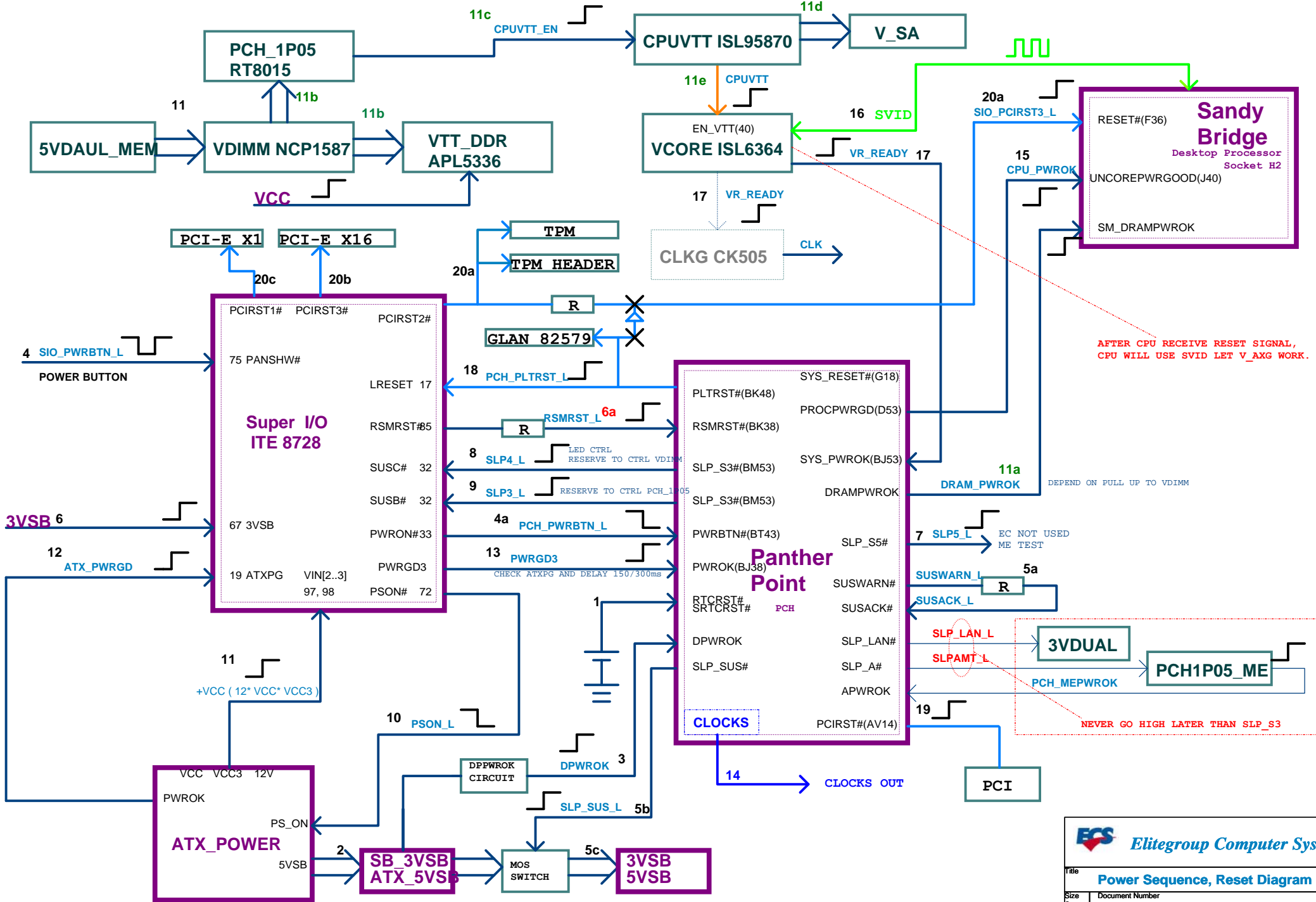
LAN INTEL 82579		
VDD3P3	3.3V	90mA
VDD1P0	1V	332mA
CTRL1P0 internal LVR Output		

SUPER I/O IT8728 FX		
3VSB	3.3V	< 6mA (S0/S1/S3/S4/S5)
VCC3	3.3V	< 10mA (S0/S1)
BAT 3.3V	3.3V	<< 2 uA (S0/S1/S3/S4/S5)

AUDIO ALC662-VD		
DVDD 3.3V	3.3V	23mA
AVDD	5V	38mA

LDO
12V
5V







**NOTE:**

Maho Bay Platform has two clock mode:

1.Integrated Clock Mode (Generate by PCH)

2.Buffer Through Mode (Generate by Clock Gen.)

If we choose Integrated Clock Mode, we should unstuff Clock Gen. circuit.

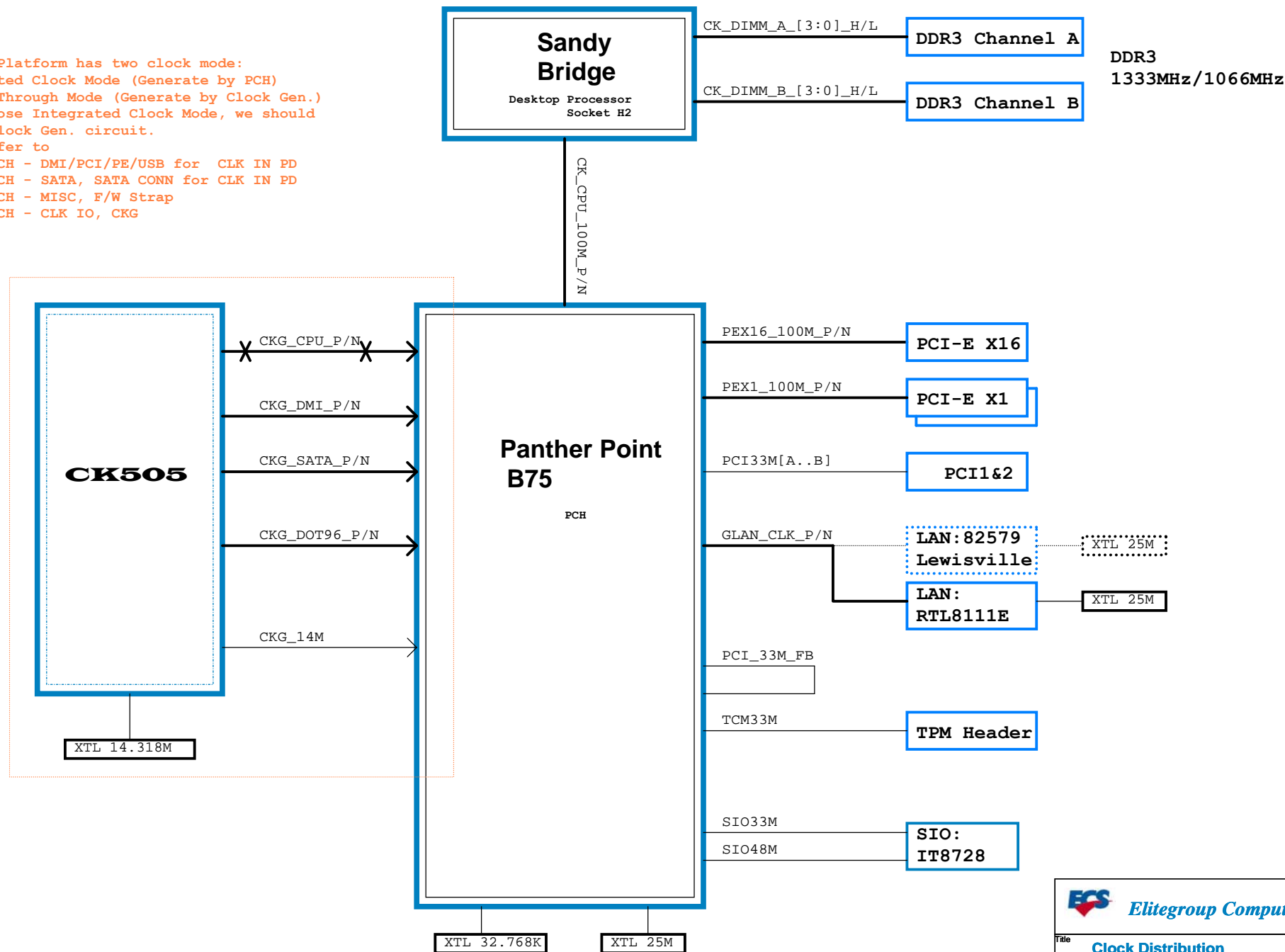
Please refer to

Page.12 PCH - DMI/PCI/PE/USB for CLK IN PD

Page.13 PCH - SATA, SATA CONN for CLK IN PD

Page.14 PCH - MISC, F/W Strap

Page.15 PCH - CLK IO, CKG



Elitegroup Computer Systems

Title  
**Clock Distribution**

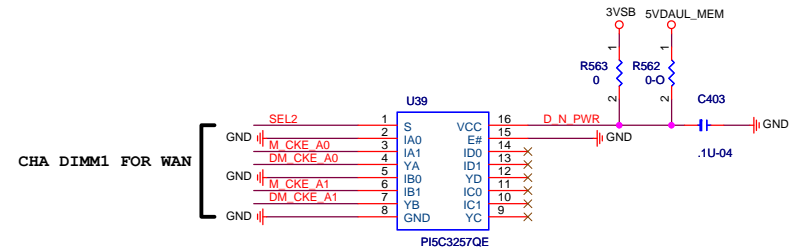
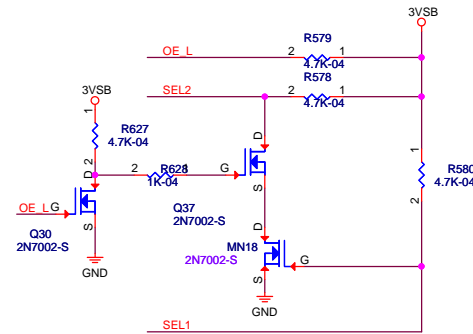
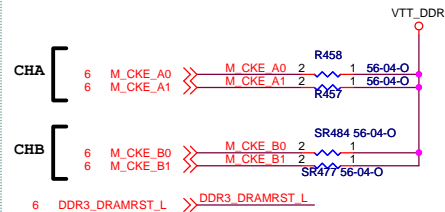
Size Custom Document Number  
**B75H2-AM-DNI**

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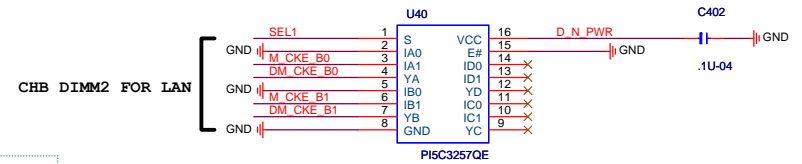
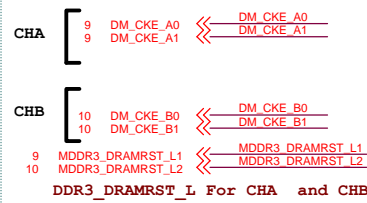
Rev  
**A**



From CPU chip

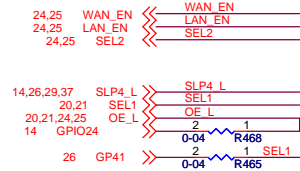


```
output to dimm
```

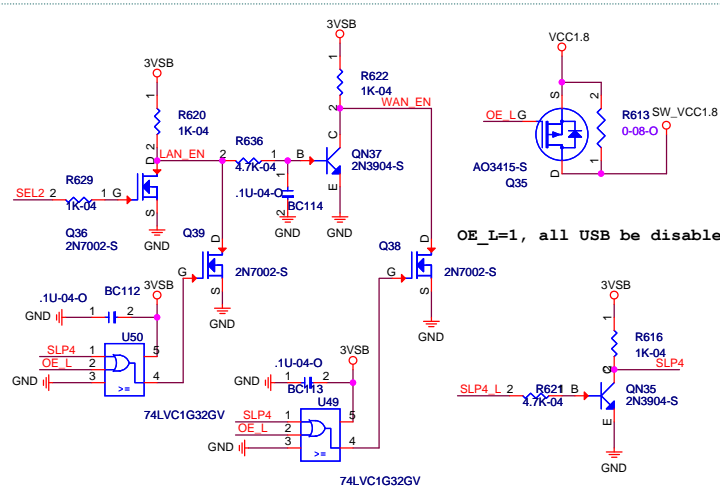


default setting SEL1=1, DIMM2 work, as LAN RAM

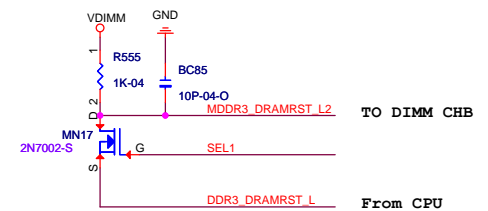
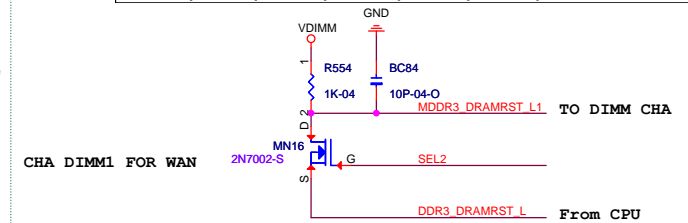
E	S	YA	YB	YC	YD	Function
H	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Disable
L	L	IA0	IB0	IC0	ID0	S = 0
L	H	IA1	IB1	IC1	ID1	S = 1



SIO GP41 reversed for BIOS detect default setting 20111215  
PCH GPIO24 as OE# GP in to confirm DUAL NET MODE



OE\_L=1, all USB be disable



DUAL-NET MODE								
	OE#							
	1		0					
SEL	SEL1	SEL2	SEL1	SEL2	SEL1	SEL2	SEL1	SEL2
	1	1	1	0	0	1	0	0
D_CKE_A0	link		open		link		NA	
D_CKE_A1	link		open		link		NA	
D_CKE_B0	link		link		open		NA	
D_CKE_B1	link		link		open		NA	
DDR3_DRAMRST_L1	link		open		link		NA	
DDR3_DRAMRST_L2	link		link		open		NA	

Y = A + B		
Input		Output
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	H

SEL1 from PCI/PCIE slot SEL#

DUAL-NET MODE CONTROL SIGNAL		
PCI SLOT	PCIEX1 SLOT	CONTROL SIGNAL
A9	A8	SLP_S3#
A11	A7	SEL#
B10	A5	PWRBTN#
B14	A6	OE#